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Datasheet for the decision
of 2 August 2012

Case Number:	T 2137/08 - 3.5.02
Application Number:	01307921.5
Publication Number:	1191696
IPC:	H03K 19/177, G06F 7/50
Language of the proceedings:	EN

Title of invention:
Programmable logic devices with function-specific blocks

Applicant:
ALTERA CORPORATION

Headword:
-

Relevant legal provisions:
EPC Art. 56

Keyword:
"Inventive step (no)"

Decisions cited:
-

Catchword:
-

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Case Number: T 2137/08 **-** 3.5.02

D E C I S I O N
of the Technical Board of Appeal 3.5.02
of 2 August 2012

Appellant: ALTERA CORPORATION
                                   101 Innovation Drive
                                   San Jose, CA 95134   (US)

Representative: Ribeiro, James Michael
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Decision under appeal: **Decision of the Examining Division of the**
                                   European Patent Office posted 24 June 2008
                                   refusing European patent application
                                   No. 01307921.5 pursuant to Article 97(2) EPC.

Composition of the Board:

Chairman: M. Ruggiu
Members: G. Flyng
                   P. Mühlens

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Summary of Facts and Submissions

I.   This appeal concerns the decision of the examining
         division refusing the European patent application
         number 01 307 921.5.

         In the contested decision, the examining division
         considered each of the requests on file at the time
         (main request and seven auxiliary requests) and found
         none to be allowable.

         Concerning the main request, the examining division
         held that claim 1 lacked novelty over the prior art
         document **US 5 825 202 (hereinafter D1).**

II.   With the statement of grounds of appeal (letter dated
         23 October 2008), the appellant submitted amended sets
         of claims of a main request and first and second
         auxiliary requests.

III.   The Board summoned the appellant to attend oral
         proceedings to be held on 2 August 2012.

         In an annex to the summons the Board set out its
         preliminary observations on the appeal, making
         reference to document D1 and to the prior art document
         WO 99/56394 (hereinafter D2), which was cited in the
         European search report.

         Considering the main request, the Board discussed the
         disclosures of D1 and D2 and questioned whether the
         subject-matter of claim 1 was novel and inventive over
         D1 or D2.

Considering the first auxiliary request, the Board noted that the amendment to claim 1 seemed to add fresh subject-matter. Furthermore, the Board noted that the gist of the feature that had been added to the claim seemed to be known from document D2.

Considering the feature added to claim 1 of the second auxiliary request, the Board expressed some doubt whether the skilled person would have inferred this feature from the application as filed. Furthermore, the Board noted that the device of D2 could apparently be configured in the manner claimed.

IV.   With a letter dated 12 June 2012 the appellant withdrew their request for oral proceedings and requested that the proceedings continue in writing. The appellant made comments in relation to document D2, arguing that claim 1 of each request was novel and inventive over D2.

V.   Oral proceedings were held on 2 August 2012. The appellant did not attend, but had requested in writing that the decision under appeal be set aside and that a patent be granted:
       –   on the basis of the Main Request filed with the grounds of appeal of 23 October 2008, or
       –   on the basis of the first auxiliary request (claim 1 filed with letter of 12 June 2012; claims 2 to 44 filed with the grounds of appeal of 23 October 2008), or
       –   on the basis of the second auxiliary request filed with the grounds of appeal of 23 October 2008.

VI.   Claim 1 of the **main request** reads as follows (feature
       references added by the Board):

       (a) "Programmable logic device circuitry comprising:
       (b) a plurality of regions of programmable logic (130);
       (c) general purpose interconnection circuitry (140)
            programmably configurable to allow outputs of
            substantially any of the regions to be applied to
            inputs of substantially any of the regions;
       (d) function-specific block ("FSB") circuitry (50);
       (e) and characterised in routing circuitry (110, 60,
            70) programmably configurable to route outputs of
            the FSB circuitry to only a subset of the regions,
       (f) wherein the routing circuitry is adapted to route
            FSB outputs for output driving by output driver
            circuitry (138) of the regions in the subset, and
            wherein the output driver circuitry of the regions
            in the subset is adapted to drive signals into the
            general purpose interconnection circuitry (140)."

       Claim 1 of the **first auxiliary request** comprises all of
       the features of main request claim 1, with the
       following additional feature at the end:

       (g1) "wherein the programmable logic device circuitry
            has no separate output drivers that are dedicated
            to the FSB outputs, the use of the output driver
            circuitry to drive the signals into the general
            purpose interconnection circuitry saving having to
            provide such output drivers that are dedicated to
            the FSB outputs".

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Claim 1 of the **second auxiliary request** comprises all
of the features of main request claim 1, with the
following additional feature at the end:

(g2) "wherein the programmable logic of the regions in
the subset that receive the FSB outputs may be
programmed to not process the FSB output signals
prior to driving the resulting signals out via the
output driver circuitry of the regions in the
subset".

VII.   The appellant has argued *inter alia* that the subject-
matter of claim 1 of the main request and of the first
and second auxiliary requests is novel with respect to
document D2 and involves an inventive step when
starting from figure 13 of document D2. Furthermore,
the appellant considers that the amendments made
according to claim 1 of the first auxiliary request and
the second auxiliary request do not add fresh subject-
matter.

Reasons for the Decision

1.   The appeal is admissible.

2.   Main request

2.1   Document D2 discloses various examples of hybrid
        integrated circuits that have a field programmable gate
        array (FPGA) portion and an application-specific
        integrated circuit (ASIC) portion (see page 1, lines 5
        to 18). These circuit portions correspond to a
        plurality of regions of programmable logic and
        function-specific block (FSB) circuitry as set out in
        features (a), (b) and (d) of claim 1 of the main
        request.

        The FPGA portion 14 is made up of an array of logic
        modules 16 with horizontal and vertical routing
        resources provided for connecting the logic modules 16
        as well as for communication with the ASIC portion 12
        (see page 2, line 16 to page 3, line 3).

        In the circuits of figures 3, 4, 7 and 9 to 14 the FPGA
        portion 14 has a multi-level hierarchical design (see
        page 3, lines 4 to 9). The FPGA portion 14 comprises
        nine logic blocks 18 having horizontal and vertical
        routing resources. Each logic block 18 comprises
        another nine logic blocks 20 having local routing
        resources. It is stated on page 8, lines numbered 2
        to 5 that "the hierarchial (sic) FPGA architecture has
        various horizontal and vertical interconnect conductors
        that programmably connect groups of logic resources at
        each level in the hierarchial design." Thus it is
        evident that these horizontal, vertical and local

routing resources amount to general purpose
interconnection circuitry that are programmably
configurable to allow outputs of substantially any of
the regions of programmable logic to be applied to
inputs of substantially any of the regions of
programmable logic (feature (c) of claim 1).

Figure 13 of D2 shows a circuit in which an
input/output module (IOM) 82 or an interface buffer 84
is placed inside the logic blocks in the FPGA portion.
FIG. 14 depicts a design similar to that of FIG. 13,
except where each IOM 82 and interface buffer 84 is
placed in the bottom row of blocks or clusters in order
to reduce the length of the dedicated interface tracks
that connect them to the ASIC portion (see paragraph
bridging pages 11 and 12).

In both figure 13 and figure 14 dedicated interface
tracks connect the IOM 82 and interface buffer 84 to
the ASIC portion 12. In the terminology of present
claim 1, these dedicated interface tracks correspond to
routing circuitry that routes outputs of the FSB
circuitry to only a subset of the programmable logic
regions, that subset being those regions of the FPGA
that have an IOM 82 or interface buffer 84 placed
inside them. Furthermore, given that the interface
buffers 84 receive and buffer signals that are output
from the FSB circuitry, they clearly constitute output
driver circuitry of the regions of the subset in the
sense of claim 1.

2.2   The appellant has argued (see letter dated 12 June 2012,
page 3, sixth paragraph) that the buffers 84 of D2 are
not "adapted to drive signals into the general purpose

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interconnection circuitry" (cf. feature (f) of claim 1). The Board is not convinced by this argument because if, as suggested in the last paragraph on page 11 of D2, the interface buffers 84 are "placed inside the logic blocks in the FPGA portion" as shown in figure 13 or 14, then these buffers would be able to be connected to the horizontal, vertical and local routing resources (i.e. programmably configurable general purpose interconnection circuitry) which connect the groups of logic resources at each level in the hierarchical design.

2.3   As set out above, in D2 the interface buffers 84 are connected to the ASIC portion 12 by dedicated interface tracks. These are not programmably configurable. Hence, the subject-matter of claim 1 of the main request may be considered to differ from the circuits depicted in figure 13 or 14 of document D2 in that the routing circuitry is programmably configurable to route outputs of the FSB circuitry to only a subset of the programmable logic regions (cf. part of feature (e)).

2.4   The appellant has argued (see letter dated 12 June 2012, page 4, second paragraph) that starting from figure 13 of D2 as the closest prior art, the problem addressed by the present invention is how to reduce cost and power consumption. The Board does not share this view. By using routing resources between the function specific block (ASIC portion) and the programmable logic regions (FPGA) that are programmably configurable, the effect achieved is to increase the flexibility of the routing. Hence, the Board sees this as being the objective problem solved by the subject-matter of claim 1 when compared to figure 13 of D2.

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2.5   Starting from the circuit of figure 13 of D2 and
        seeking to increase the flexibility of the routing
        between the ASIC portion and the FPGA portion, the
        Board considers that it would be obvious for the
        skilled person to use a FPGA-ASIC routing channel such
        as is disclosed in various other embodiments of D2 (see
        figures 4, 5 and 7 to 10). As set out in the third
        paragraph on page 9 of D2, an FPGA-ASIC routing channel
        would facilitate the distribution of the signals
        between the ASIC portion and the FPGA portion, or in
        other words would increase the flexibility of the
        routing. Also as set out in that paragraph, the FPGA-
        ASIC routing channel may be either hardwired or contain
        a plurality of programming elements 42. Clearly such
        programming elements would be programmably configurable
        to route outputs of the FSB circuitry to only a subset
        of the programmable logic regions of the FPGA portion,
        that being their very purpose.

2.6   The Board concludes that in the manner set out above
        the person skilled in the art would come to the
        subject-matter of claim 1 of the main request without
        involving an inventive step, Article 56 EPC.

3.   First auxiliary request

3.1   According to feature (g1) of claim 1 of the first
        auxiliary request, "the programmable logic device
        circuitry has no separate output drivers that are
        dedicated to the FSB outputs, the use of the output
        driver circuitry to drive the signals into the general
        purpose interconnection circuitry saving having to

provide such output drivers that are dedicated to the
FSB outputs" (emphasis added).

In the application as filed it is stated that use of
the output drivers of the logic elements "saves having
to provide separate output drivers that are dedicated
to the FSB outputs" (see the published application,
EP 1 191 696 A2, paragraph [0050]). This does not seem
to necessarily imply that the <u>programmable logic device
circuitry</u> has no separate output drivers that are
dedicated to the FSB outputs. It might rather imply
that there is no need to provide dedicated FSB output
drivers that are separate from the programmable logic
circuitry. Hence, the Board considers that the wording
of feature (g1) might add fresh subject-matter,
contrary to Article 123(2) EPC.

3.2   Notwithstanding the above, the Board considers that in
        the device of figures 13 and 14 of document D2, by
        configuring a certain number of programmable logic
        modules of the FPGA as buffers for signals emanating
        from the ASIC, into the horizontal and vertical routing
        resources of the FPGA, it is possible to avoid separate
        interface buffers dedicated for the ASIC signals, such
        as the separate interface buffers 26 that are used in
        other embodiments (see figures 4, 7, 9, 10 and 11).
        Hence, the Board finds that the gist of feature (g1) is
        known from the circuit in figure 13 or 14 of D2 and
        that the subject-matter of claim 1 of the first
        auxiliary request lacks an inventive step for the same
        reasons as given above for the main request.

3.3   The appellant has argued that the buffers 84 in figures
        13 and 14 are functionally dedicated to the ASIC

outputs in the sense that they provide no driving for
the logic blocks in which they are placed (see page 4
of the letter dated 12 June 2012, third paragraph under
the heading arguments in relation to the first
auxiliary request). However this does not address the
point that these buffers are not separate from the FPGA.
Furthermore, when introducing an FPGA-ASIC routing
channel to increase flexibility the buffers 84 would no
longer be dedicated to particular ASIC outputs and
hence, when a given buffer is not needed for driving
ASIC outputs, it would be obvious to the person skilled
in the art to configure it to buffer signals emanating
from within the FPGA.

4.   Second auxiliary request

4.1   According to feature (g2) of claim 1 of the second
        auxiliary request, "the programmable logic of the
        regions in the subset that receive the FSB outputs may
        be programmed to not process the FSB output signals
        prior to driving the resulting signals out via the
        output driver circuitry of the regions in the subset".

4.2   The Board has some doubts whether the skilled reader
        would indeed infer this "negative" alternative (*may be
        programmed to not process the FSB output signals*) just
        from the disclosure of the opposite "positive"
        alternative in paragraphs [0054] and [0055] of the
        application as filed (*may/can also be used to process
        the FSB output signals*).

4.3   Notwithstanding the above, the Board considers that in
        the device of figures 13 and 14 of document D2, it
        would be an obvious possibility when programming the

FPGA to send a given signal output from the ASIC
portion to parts of the FPGA other than the particular
logic block in which the buffer that receives the ASIC
signal is located. Thus, it would be obvious to
configure the logic block containing the buffer so that
it does not process the ASIC signal before it is
buffered, but passes it on to other logic blocks
unprocessed. Hence the Board finds that the subject-
matter of claim 1 of auxiliary request 2 is obvious in
view of the prior art.

5.   Conclusion

As none of the appellant's requests could form a basis
for the grant of the patent, the appeal has to be
dismissed.

Order

For the above reasons it is decided that:

The appeal is dismissed.

The Registrar: The Chairman:

U. Bultmann   M. Ruggiu

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