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Datasheet for the decision of 11 May 2012

Case Number: T 2116/08 - 3.5.06

Application Number: 03798250.1

Publication Number: 1546869

IPC: G06F 9/38, G06F 9/312, G06F 9/45

Language of the proceedings: EN

Title of invention:
Apparatus, method, and compiler enabling processing of load immediate instructions in a very long instruction word processor

Applicant:
Silicon Hive B.V.

Headword:
VLIW instruction/SILICON HIVE

Relevant legal provisions (EPC 1973):
EPC Art. 56

Keyword:
"Inventive step - yes (after amendment)"

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Beschwerdekammern | Boards of Appeal | Chambres de recours

Case Number: T 2116/08 - 3.5.06

D E C I S I O N
of the Technical Board of Appeal 3.5.06
of 11 May 2012

Appellant: (Applicant)
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Decision under appeal: **Decision of the Examining Division of the European Patent Office posted 12 June 2008 refusing European application No. 03798250.1 pursuant to Article 97(2) EPC.**

Composition of the Board:

Chairman: D. H. Rees
Members: M. Müller
W. Sekretaruk

Summary of Facts and Submissions

I. The appeal lies against the decision of the examining division, with written reasons dated 12 June 2008, to refuse the European patent application 03798250.1 for lack of inventive step over the following documents

D1: EP 0 886 210 A2
D3: US 6 023 756 A.

II. An appeal was filed on 19 August 2008 and the appeal fee was paid on the same day. A statement of grounds of appeal was filed on 20 October 2008 along with two sets of claims according to a main and an auxiliary request.

III. With summons to oral proceedings, the board gave its preliminary opinion raising objections under Article 52 (2,3) EPC and Article 84 EPC 1973 but considering that the claims of the auxiliary request on file showed an inventive step when construed in the light of the description. The board also indicated that the oral proceedings could be avoided if suitably amended claims were filed.

IV. In response to the summons, with telefax dated 8 March 2012, the appellant withdrew the main request and filed new claims and description pages according to the request which, albeit still being referred to as "auxiliary request" by the appellant, constitutes the sole remaining request. Explaining this request, the appellant refers to description pages and drawings "as originally filed". Noting that the application had originally been filed as an International application, the board takes this to refer to description pages and

drawings *as published* by the International Bureau on which, according to the request for entry into the regional phase, the proceedings before the EPO should be based. The board cancelled the scheduled oral proceedings.

V. The board thus takes the appellant's request to be that the decision under appeal be set aside and that a patent be granted based on the following documents:

Claims, numbers

1-4	as filed on 8 March 2012

Description, pages

2, 6, 7, 10, 11	as published
3	labelled "AUXILIARY REQUEST", as filed on 20 October 2008
1, 4, 5, 5a, 8, 9	as filed on 8 March 2012

Drawings, numbers

1/4-4/4	as published

VI. The independent claims 1 and 4 read as follows:

"1. A VLIW processing apparatus for processing data, based on control signals generated from a set of instructions being grouped in a VLIW instruction (401) and being executed in parallel, comprising:

a plurality of first issue slots (UC_0, UC_1, UC_2, UC_3), wherein each first issue slot comprises a plurality of functional units (FU_{20}, FU_{21}, FU_{22}), the plurality of first issue slots being controlled by a set of control words, corresponding to the set of instructions,

a dedicated first register file (RF_2) only for storing an immediate value (IMV1), the dedicated first

register file (RF_2) being accessible by the plurality of first issue slots (UC_0-UC_3),

characterized by a dedicated second issue slot (UC_4) arranged for loading a dedicated instruction (IMM) consisting of an immediate value and passing the immediate value to the dedicated register file (RF_2), wherein the dedicated second issue slot (UC_4) comprises a single dedicated function unit (IMU) arranged for only executing the dedicated instruction (IMM), and wherein the VLIW instruction is a compressed VLIW instruction, comprising dedicated bits for encoding NOP operations.

4. A method for processing data, said method comprising the following steps:

- storing input data in a register file (RF_0, RF_1);
- processing data retrieved from the register file (RF_0, RF_1) based on control signals generated from a set of instructions being grouped in a VLIW instruction (401) and being executed in parallel, using a plurality of first issues slots (UC_0, UC_1, UC_2, UC_3) controlled by a set of control words being generated from the set of instructions;

characterized by

loading a dedicated instruction (IMM) consisting of an immediate value (IMV1) into a dedicated second issue slot (UC_4),

executing the dedicated instruction by a dedicated functional unit (IMU) associated to the dedicated second issue slot (UC_4), and

storing the immediate value (IMV1) in a dedicated first register file (RF_2) which is accessible by the dedicated second issue slot and by the plurality of first issue slots, and wherein the VLIW instruction is

a compressed VLIW instruction, comprising dedicated bits for encoding NOP operations."

Reasons for the Decision

The Invention

1. In the context of VLIW processors the application relates to the efficient encoding and decoding of instructions with large immediate arguments.

1.1 The VLIW processor as claimed is specified to comprise a plurality of "first issue slots", each having a plurality of "functional units" - to execute the multiple VLIW instructions (see description, p. 2, lines 5-7) -, a dedicated "first register" accessible by the "first issue slots", and especially a "dedicated second issue slot".

1.2 This second issue slot is set up to deal with only "one type of instruction" (p. 6, lines 21-23), namely a "dedicated instruction (IMM) consisting of an immediate value" to be loaded into the dedicated register. The second issue slot has a dedicated functional unit for performing the dedicated loading instruction.

2. According to established jurisprudence of the boards of appeal, the claimed instruction "consisting of an immediate value" is interpreted to comprise *nothing but* an immediate value and thus neither an operation code (opcode), in accordance with the description (see p. 4 as originally published, lines 16-18), nor any other argument such as a target register index. The VLIW pro-

cessor will thus interpret any value in the IMM instruction as an immediate value to be moved into the dedicated register. The possibility that for a given VLIW instruction no IMM instruction is to be executed is expressed by the claimed "bits for encoding NOP operations": A value of '0' in the bit position corresponding to the IMM instruction indicates that the value in the IMM field is to be ignored, a value of '1' indicates that the IMM value is to be loaded into the dedicated register.

The Prior Art

3. D1 discloses a VLIW processor with at least two operations per VLIW instruction and correspondingly two "issue slots" (instruction decoders 24 and 25 in fig. 4).

3.1 Each issue slot has its operations executed by a dedicated operation unit (fig. 4, nos. 37 and 38) which is capable of executing two types of operations by respective "functional units" (see col. 11, lines 28-44; esp. arithmetic logic operations and multiplication).

3.2 D1 discloses several types of (load) instructions for storing a constant (*i.e.* an immediate value) in a dedicated register, under the control of a dedicated component, called a constant register control unit (fig. 4, nos. 32 and 36; col. 9, lines 6-23 and col. 10, lines 53-57). According to a format code (fig. 2a-2d, no. 51) the immediate value to be stored is held in field 52 of an instruction in case of a 4 bit constant, and in field 52 in combination with fields 53-55 (1st operand) or 56-58 (2nd operand) in case of a 16 bit constant

(col. 9, lines 6-24; figs. 2B and 2C, format codes "0", "1", "4" or "5"). The dedicated register is accessible by the functional units (nos. 36-38; cf. col. 11, lines 22-27; col. 13, lines 18-29).

4. D3 refers, in its section on prior art, to a VLIW instruction set providing, *inter alia*, a dedicated "small instruction" for an "immediate (IMM) instruction" which is "to set an operand value to the general register" (cf. col. 1, lines 39-43 and 48-49; fig. 1, no. 405). No further details about the format or the execution of this immediate instruction are disclosed. Other parts of D3 are not addressed in the decision under appeal and indeed are of little relevance for the inventive step of the claimed invention.

Articles 123 (2) EPC and 84 EPC 1973

5. The board is satisfied that the amendments comply with Article 123 (2) EPC and that the pending claims comply with Article 84 EPC 1973.

Articles 54 and 56 EPC 1973

6. It is common ground that D1 constitutes the only suitable starting point for the assessment of inventive step put forward by the examining division.

6.1 Independent claims 1 and 4 differ from D1 in disclosing a dedicated (second) issue slot with a dedicated functional unit that is arranged for executing the dedicated instruction consisting of an immediate argument (cf. point 2 above and grounds of appeal, points I.2.4 and I.3.4.1). In essence, this also corresponds

to the analysis according to the decision under appeal (p. 3, point 11.05).

6.2 These differences solve the objective technical problem of providing an efficient way of handling immediate values by a VLIW processor.

6.3 The decision under appeal argues (p. 3, point 11.07) that it is "well known in the art" to use "a dedicated issue slot for simplifying instruction decoding" and refers to D3 by illustration.

6.4 The board agrees with this statement but is not of the opinion that it is sufficient to imply or suggest reducing the pertinent instruction to the immediate operand value alone, without an explicit opcode. The specific disclosure of D3 must therefore be considered.

7. D3 discloses a VLIW system with a dedicated immediate instruction (IMM) but does not provide any detail as to the structure of the immediate instruction or how it is executed. Specifically, D3 discloses neither that the immediate instruction lacks an opcode, nor that it is executed by a dedicated issue slot with a dedicated functional unit. Further, the board agrees with the appellant's submission that instructions normally have opcodes and that there is no basis to assume that VLIW instructions without an opcode are common in the art. In particular, D3 does not suggest such instructions.

7.1 An immediate instruction as generally understood is any instruction with an operand containing the *value* of data to be processed rather than its *address*. An immediate instruction may have more than one operand,

for example the instruction to load an immediate value into one of several registers.

7.2 D3 discloses that "[t]he IMM instruction is to set an operand value to the general register" (col. 1, lines 48-49). Elsewhere in the pertinent paragraph D3 does not mention a specific general register in the singular form. Rather, in the context of the "load/store instruction", several "internal general registers" are mentioned, and in the context of the "ALU instruction" reference is made to "the internal general registers mentioned above" (col. 1, lines 44-48). In the board's view the skilled person would thus interpret D3 as disclosing an IMM instruction for loading an operand value into one of the internal general registers, *i.e.* an IMM instruction with two operands. Already for that reason D3 does not disclose an IMM instruction "consisting of [only] an immediate value".

7.3 The board is of the opinion that the skilled person might consider providing, in addition, an IMM instruction for moving an operand value into a dedicated register. This instruction could leave the register implicit and would thus need only one operand (implicit addressing mode). According to common practice however these two IMM instructions would be distinguished by their opcodes.

7.4 The board also notes that D1 discloses immediate instructions with operand values of different bit length (cf. col. 9, lines 8-23; figs. 2B and 2C). Again, the board considers that it would be normal practice to use different opcodes to distinguish between these variants.

8. The board thus concludes that it would not be obvious for the skilled person starting from D1, even in view of D3, to set up a VLIW instruction set and the corresponding processor or processing method in such a way that they support an IMM instruction consisting of nothing but an immediate value, in particular without an opcode. Claims 1 and 4 thus show the required inventive step over D1 in combination with D3.

9. Since no other possible starting point for considering the inventive step has been put forward by the examining division or is apparent to the board, the board concludes that Article 56 EPC 1973 is satisfied.

Order

For these reasons it is decided that:

1. The decision under appeal is set aside.

2. The case is remitted to the department of first instance with the order to grant a patent based on the following documents:

Claims, numbers	
1-4	as filed on 8 March 2012
Description, pages	
2, 6-11	as published
3	labelled "AUXILIARY REQUEST", as filed on 20 October 2008
1, 4, 5, 5a, 8, 9	as filed on 8 March 2012
Drawings, numbers	
1/4-4/4	as published

The Registrar: The Chairman:

B. Atienza Vivancos D. H. Rees