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Case Number: T 1990/08 - 3.4.03

Application Number: 00971735.6

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Title of invention:
Driving Circuit and Display

Applicant:
Panasonic Corporation

Opponent:
-

Headword:
-

Relevant legal provisions:
-

Relevant legal provisions (EPC 1973):
EPC Art. 56
EPC R. 67

Keyword:
"Inventive step - yes"
"Reimbursement of the appeal fee - no"

Decisions cited:
J 0003/06, J 0010/07

Catchword:
See point 7.3

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Beschwerdekammern | Boards of Appeal | Chambres de recours

Case Number: T 1990/08 **-** 3.4.03

D E C I S I O N
of the Technical Board of Appeal 3.4.03
of 6 March 2012

Appellant: (Applicant)
Panasonic Corporation
1006, Oaza Kadoma
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Representative:
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Decision under appeal: **Decision of the Examining Division of the European Patent Office posted 27 May 2008 refusing European patent application No. 00971735.6 pursuant to Article 97(2) EPC.**

Composition of the Board:

Chair: T. Karamanli
Members: T. Häusser
E. Wolff

Summary of Facts and Submissions

I. The appeal concerns the decision of the examining division posted on 27 May 2008 to refuse European patent application No. 00 971 735 for added subject-matter, Article 123(2) EPC (main and auxiliary requests), lack of clarity, Article 84 EPC (main request), and lack of inventive step, Article 56 EPC (main request) in view of the following documents:

D1: JP-A-3 183 211 with corresponding Patent Abstracts of Japan,
D4: FR-A-2 762 705.

II. Reference is also made to the following document:

D1': translation of published patent JP-B-2 541 325, which corresponds to the application D1

III. At oral proceedings before the board the appellant requested that the decision under appeal be set aside and that a patent be granted in the following version:

- claims 1 to 3 according to the sole request, filed with letter of 3 February 2012,
- description pages 1 to 4, 4a, 4b, 5, 17 to 58, filed during the oral proceedings of 6 March 2012,
- drawing sheets 1/14 to 14/14, filed during the oral proceedings of 6 March 2012.

The appellant further requested that the appeal fee be refunded.

IV. The wording of claim 1 reads as follows:

"A plasma display device, comprising:
a display panel (1) including a capacitive load (Cp) composed of a plurality of electrodes (11, 12, 13); and
a driving circuit (4) configured to output a driving pulse to drive said capacitive load (Cp) in said display panel (1);
said driving circuit (4) comprising:
a first voltage source (V1; V31) for supplying a first voltage for causing said driving pulse to rise;
a second voltage source for supplying a second voltage lower than said first voltage for causing said driving pulse to fall;
an electrical circuit connected to a pulse supply path for supplying said driving pulse to said capacitive load (Cp), and having
first switching means (Q1; Q31) having one end connected to the first voltage source (V1; V31);
second switching means (Q2; Q32) having one end connected to the second voltage source;
an interconnection portion (L1, N1, L2; L31, N1, L32) having one end connected to the other end of said first switching means (Q1; Q31) and the other end connected to the other end of said second switching means (Q2; Q32), wherein said first switching means (Q1; Q31) and said second switching means (Q2; Q32) are configured such that said interconnection portion (L1, N1, L2; L31, N1, L32) is connected only to either one of said first voltage source (V1; V31) and said second voltage source at the same time;

an inductance element (L) such as a recovering coil having one end connected to the interconnection portion (L1, N1, L2; L31, N1, L32);
a recovering capacitive element (Cr) such as a recovering capacitor for recovering charges from said capacitive load (Cp);
a first one-way conductive element (D1) such as a diode having one end connected to the other end of the inductance element (L);
third switching means (Q3) such as a transistor having one end connected to the capacitive recovering element (Cr) and the other end connected to said first one-way conductive element (D1);
a second one-way conductive element (D2) such as a diode having one end connected to the other end of the inductance element (L); and
fourth switching means (Q4) such as a transistor having one end connected to said capacitive recovering element (Cr) and the other end connected to said second one-way conductive element (D2); wherein
the capacitive load (Cp) of said display panel (1, Cp) is connected to said interconnection portion (L1, N1, L2; L31, N1, L32), and
said second switching means (Q2; Q32) is configured to be turned on before the potential (Psu) of said display panel (Cp) attains the potential of said second voltage source with respect to one operation phase of said driving circuit (4), and at substantially the same time, said fourth switching means (Q4) are configured to be turned off,
characterized by
a first capacitor (C1; C31) connected in parallel to said first switching means (Q1; Q31) which is configured to reduce the resonance frequency of LC

resonance by a parasitic capacitance of said first switching means (Q1; Q31) and an inductance component of said interconnection portion (C1, N1, L2; L31, N1, L32), and
a second capacitor (C2; C32) connected in parallel to said second switching means (Q2; Q32) which is configured to reduce the resonance frequency of LC resonance by a parasitic capacitance of said second switching means (Q2, Q32) and an inductance component of said interconnection portion (L1, N1, L2; L31, N1, L32); wherein
the capacitance of said first capacitor (C1; C31) is five to ten times as much as that of the parasitic capacitance of said first switching means (Q1; Q31), and
the capacitance of said second capacitor (C2; C32) is five to ten times as much as that of the parasitic capacitance of said second switching means (Q2; Q32)."

V. The appellant argued essentially as follows:

(a) Inventive step

The closest prior art was document D4 from which the subject-matter of claim 1 differed in comprising the characterizing part of claim 1. LC resonance caused by parasitic capacitances and leading to unwanted high frequency electromagnetic wave radiation was the problem. The effect of the features referred to in the characterizing part of claim 1 was to suppress these high frequency electromagnetic waves.

Neither document D1, which proposed to suppress switching noise, nor document D4 recognized the problem, and interpreting the prior art in full knowledge of the problem and its solution could only be criticized as an *ex post facto* analysis.

The problem addressed in document D4 was different from that solved by the invention: whereas the LC resonance described in the invention occurred whenever a switch changed from an off state to an on state, the unwanted rash current in D4 occurred at specific instants T12 and T14 due to a finite "on" resistance of the transistors and had noise as an unwanted consequence. In document D4 the rash current as such was considered to be the problem and a solution to that problem was provided in that document.

The decision under appeal also failed to clarify why the skilled person would consider applying the teaching of D1 to that of D4, especially as document D1 was also concerned with a different problem from the invention, namely the moderation of switching noise.

Even if the skilled person were to consider combining the teachings of documents D1 and D4, he would not arrive at the claimed subject-matter. In particular, *large capacitances* were needed to address the problems of D1 and D4. However, according to the invention such large capacitances were not used but rather capacitances which were only five to ten times larger than the parasitic capacitances of the switching means. In this way it was avoided that the voltage change was too slow which would cause unstable plasma discharge.

The present invention was therefore not rendered obvious by documents D1 and D4, whether taken alone or in combination.

(b) Reimbursement of the appeal fee

According to the appellant there was a dispute with the examining division regarding the content of D1. Document D1 was concerned with moderating the steep change of current in a circuit, which might otherwise cause switching noise like "ground bounce". Furthermore, specific parts of document D1 were cited by the appellant on page 3 of the letter of 10 August 2007 indicating that a large amount of current needed to be flushed through the capacitors in order to cope with the problem of switching noise. On the other hand, in the decision under appeal it was merely asserted in section 1.1.6 under the point "Ad (5)" that no basis could be identified in document D1 for the statement that far larger capacitances were needed for addressing the problem mentioned in D1. Following the Guidelines C-IV, 6.4 (in the version then in force) the examining division should therefore have provided a translation of the document D1, irrespective of whether the applicant had requested a translation or not.

By not providing a translation of D1 the examining division committed a substantial procedural violation since the inventive step arguments of the examining division were based on its wrong appreciation of document D1. Provision of the translation would have led to a correct appreciation so that no appeal would have had to be filed. Therefore a refund of the appeal fee was justified, even if the decision under appeal

was not only based on lack of inventive step but also on other grounds as far as the claims of the requests then on file were concerned.

Reasons for the Decision

1. The present decision was taken after the revised European Patent Convention entered into force on 13 December 2007. Since the application in suit was pending at that time, the Board applied the transitional provisions in accordance with Article 7(1), second sentence, of the Act revising the EPC of 29 November 2000 (hereinafter "the Revision Act") and the decision of the Administrative Council of 28 June 2001 on the transitional provisions under Article 7 of the Revision Act (Special edition No. 1, OJ EPO 2007, 197) and the decision of the Administrative Council of 7 December 2006 amending the Implementing Regulations to the EPC 2000 (Special edition No. 1, OJ EPO 2007, 89). Articles and rules of the revised EPC and of the EPC valid until that time are cited in accordance with the "Citation Practice" (see the 14th edition of the European Patent Convention, page 6).

2. Admissibility

The appeal is admissible.

3. Amendments

Claim 1 is based on original claims 1, 2, 9 to 13, 15 and the description as originally filed (page 19, lines 20-22; page 22, line 7 – page 23, line 14;

page 25, lines 12-17; page 27, lines 1-6; page 29, lines 8-13).

Dependent claims 2 to 3 are based on original claim 5 and the description as originally filed (page 22, lines 7-11).

The description has been brought into conformity with the amended claims and supplemented with an indication of the relevant content of the prior art without extending beyond the content of the application as filed.

Accordingly, the board is satisfied that the amendments comply with the requirements of Article 123(2) EPC.

4. Novelty

4.1 Document D4 discloses (see Figures 14 and 15, page 16, fourth paragraph – page 19, first paragraph) a circuit comprising switches S11 to S14, diodes D11 to D12, an energy recovery coil L1, an energy recovery capacitor C10, and an electrostatic capacitance C2 of a plasma display panel as load connected to the terminal TP1. A terminal TP2 is connected to a power supply for providing a sustained discharge pulse voltage VS.

To cause a pulse rise, the switch S14 which has been clamping the voltage at the terminal TP1 to the ground voltage is turned off while the switch S11 is turned on thereby causing current to flow from the capacitor C10 through the switch S11, the diode D11 and the coil L1. Then the switch S13 is turned on to clamp the voltage at the terminal TP1 to the voltage VS. To cause a pulse

fall, the switches S11 and S13 are turned off while the switch S12 is turned on. Then the switch S14 is turned on to clamp the voltage at the terminal TP1 to the ground voltage. A voltage jump ΔV is caused when the clamping circuit is turned on at the rising and falling edges of the pulse.

4.1.1 Using the wording of claim 1, document D4 discloses a plasma display device, comprising:
a display panel including a capacitive load (C2) composed of a plurality of electrodes (implicit); and
a driving circuit configured to output a driving pulse to drive said capacitive load (C2) in said display panel;
said driving circuit comprising:
a first voltage source (power supply connected to terminal TP2) for supplying a first voltage (VS) for causing said driving pulse to rise;
a second voltage source (ground) for supplying a second voltage lower than said first voltage for causing said driving pulse to fall;
an electrical circuit connected to a pulse supply path for supplying said driving pulse to said capacitive load (C2), and having
first switching means (S13) having one end connected to the first voltage source;
second switching means (S14) having one end connected to the second voltage source;
an interconnection portion having one end connected to the other end of said first switching means (S13) and the other end connected to the other end of said second switching means (S14) (see the connection between the switches S13 and S14 in Figure 14), wherein said first switching means (S13) and said second switching means

(S14) are configured such that said interconnection portion is connected only to either one of said first voltage source and said second voltage source at the same time (at the end of pulse rise to VS and at the end of pulse fall to ground, see switches S13 and S14 in Figure 15);
an inductance element (L1) such as a recovering coil having one end connected to the interconnection portion;
a recovering capacitive element (C10) such as a recovering capacitor for recovering charges from said capacitive load (C2);
a first one-way conductive element (D11) such as a diode having one end connected to the other end of the inductance element (L1);
third switching means (S11) such as a transistor having one end connected to the capacitive recovering element (C10) and the other end connected to said first one-way conductive element (D11);
a second one-way conductive element (D12) such as a diode having one end connected to the other end of the inductance element (L1); and
fourth switching means (S12) such as a transistor having one end connected to said capacitive recovering element (C10) and the other end connected to said second one-way conductive element (D12); wherein
the capacitive load (C2) of said display panel is connected to said interconnection portion, and
said second switching means (S14) is configured to be turned on before the potential of said display panel (C2) attains the potential of said second voltage source with respect to one operation phase of said driving circuit, and at substantially the same time,

said fourth switching means (S12) are configured to be turned off (see switches S12 and S14 in Figure 15).

4.1.2 Document D4 does not disclose the characterizing features of claim 1, namely

(1) a first capacitor connected in parallel to said first switching means which is configured to reduce the resonance frequency of LC resonance by a parasitic capacitance of said first switching means and an inductance component of said interconnection portion, and

(2) a second capacitor connected in parallel to said second switching means which is configured to reduce the resonance frequency of LC resonance by a parasitic capacitance of said second switching means and an inductance component of said interconnection portion; wherein

(3) the capacitance of said first capacitor is five to ten times as much as that of the parasitic capacitance of said first switching means, and

(4) the capacitance of said second capacitor is five to ten times as much as that of the parasitic capacitance of said second switching means.

4.1.3 The subject-matter of claim 1 is therefore new over document D4.

4.2 None of the remaining prior art documents on file is closer to the subject-matter of claim 1 than document D4. Claims 2 to 3 are dependent on claim 1 providing further limitations.

Accordingly, the subject-matter of claims 1 to 3 is new (Article 52(1) EPC and Article 54(1) EPC 1973).

5. Inventive step

5.1 The plasma display device described in document D4 with respect to Figures 14 and 15 of that document is structurally closest to the subject-matter of claim 1 and is therefore regarded to be the closest state of the art.

5.2 The subject-matter of claim 1 differs from the closest state of the art in comprising features (1) to (4) (see point 4.1.2 above).

5.3 On switching the circuit emits electromagnetic wave radiation at the resonance frequency of the LC resonance caused by a parasitic capacitance of the first or second switching means and an inductance component of the interconnection portion. The effect of features (1) to (4) is to reduce that resonance frequency thereby suppressing high frequency electromagnetic wave radiation (see the description of the application, page 4, second paragraph; page 31, second paragraph). The objective technical problem is therefore to reduce high frequency electromagnetic wave radiation.

5.4 In the decision under appeal (see in particular points 1.1.1 to 1.1.4 of the Reasons for the Decision) the examining division stated that document D4 was concerned with eliminating the surge currents at instants T12 and T14 which were responsible for generating noise. Furthermore, it was held that document D1 disclosed the occurrence of switching noise caused by switching either one of the transistors to

the ON state. Due to the similarity of the circuit and the technical problem in D1 with the circuit and technical problem of D4 and of the claimed invention, the skilled person would consider document D1 when attempting to solve the posed problem. D1 disclosed that the switching noise would be suppressed by connecting a capacitor in parallel to each of the transistors. The skilled person would understand that the capacitor needed to be significantly bigger than the drain-source capacitance of the transistors in order to achieve the desired effect but not too big as otherwise the voltage change would become too slow. The examining division concluded that the skilled person would thus combine the teachings of D4 and D1 to arrive at the subject-matter of claim 1, which therefore lacked inventive step.

5.4.1 In relation to the closest state of the art, i.e. the prior art described with respect to Figures 14 and 15, document D4 is concerned with power loss and noise generation caused by ***surge currents*** at instants T12 and T14 when the voltage is clamped to the voltage VS of a voltage source and to the ground voltage, respectively (D4, page 16, line 16 – page 19, line 2 and page 21, line 32 – page 22, line 3).

It is not described in document D4 what is meant by "noise", in particular there is no disclosure that it relates to electromagnetic wave radiation. Furthermore, the high frequency electromagnetic wave radiation to be reduced according to the invention is not caused by surge currents but occurs whenever a switch is changed from an off to an on state thereby leading to LC resonance generated by the drain-source capacitance and

the inductance component of the lines (see the description of the application, page 3, paragraph 3).

In the board's view, the skilled person would therefore not be led by the disclosure of document D4 to consider solving the objective technical problem. Rather, starting from the closest state of the art he would at most be led to reducing power loss and noise generation caused by surge currents, e.g. by providing a driving circuit according to the first embodiment of D4, described with respect to Figures 1 and 2 (see D4, page 35, line 4 – page 43, line 20).

5.4.2 Document D1 relates to an output buffer circuit in which a load capacity 8 is charged or discharged depending on the logical level of a data input terminal 4 (see the abstract). Document D1 is concerned with switching noise occurring whenever the logical level of an output changes. The change of the logical level of the output leads to a current change which in turn induces a voltage in parasitic inductances of the output buffer circuit. These induced voltages are called "switching noise" and may have adverse effects on the circuit operation and may even cause malfunction of the circuit (see the description in relation to Figure 4 in document D1').

Document D1 is therefore not concerned with reducing high frequency electromagnetic wave radiation and would therefore not be considered relevant by the skilled person when attempting to solve the posed objective technical problem.

5.4.3 Hence the subject-matter of claim 1 involves an inventive step over document D4, also in combination with document D1.

5.5 None of the other prior art documents on file contains a teaching that would lead the skilled person in an obvious way to the subject-matter of claim 1. Nor is the subject-matter of claims 2 to 3 considered obvious as these claims are dependent on claim 1.

Accordingly, the subject-matter of claims 1 to 3 involves an inventive step over the available state of the art (Article 52(1) EPC and Article 56 EPC 1973).

6. Other requirements of the EPC and conclusion

The description has been brought into conformity with the amended claims in order for them to comply with the requirements of Article 84 EPC 1973. Furthermore, the description has been supplemented with an indication of the relevant content of the prior art to comply with the requirements of Rule 27(1)(b) EPC 1973, which is to be applied in the present case since the present application was filed before 13 December 2007 and Rule 27(1)(b) EPC is linked to Article 83 EPC 1973 which continues to apply in the present case in accordance with Article 7(1), second sentence, of the Revision Act (loc. cit.) and Article 1, No. 1, of the decision of the Administrative Council of 28 June 2001 on the transitional provisions under Article 7 of the Revision Act (loc. cit.) (see in detail case J 3/06, Reasons, point 3).

In view of the above the sole request is allowable.

7. Request for reimbursement of the appeal fee

7.1 The appellant argued that the examining division committed a substantial procedural violation by not providing a translation of document D1, which justified the reimbursement of the appeal fee.

7.2 First, the board has to determine whether the provisions of Rule 67, first sentence, EPC 1973 or Rule 103(1)(a) EPC apply to the present case as far as the requirements for reimbursement of the appeal fee are concerned.

An application that was filed before 13 December 2007 is, within the meaning of Article 2 of the decision of the Administrative Council of 7 December 2006 amending the Implementing Regulations to the European Patent Convention 2000 (loc. cit.), subject to the provisions of the revised EPC if the article of the European Patent Convention to which the implementing regulation relates is applicable from the time the revised EPC entered into force (see in detail case J 3/06, Reasons, point 3).

Rule 103(1)(a) EPC is linked to Articles 109 and 111 EPC (see also decision J 10/07, Reasons, point 7). According to Article 1 of the decision of the Administrative Council of 28 June 2001 on the transitional provisions under Article 7 of the Revision Act (loc. cit.), the provisions of Articles 109 and 111 EPC do not however apply to the present application which was pending at the time of their entry into force (see point 1 above). Therefore, in accordance with

Article 7(1), second sentence, of the Revision Act (loc. cit.), Articles 109 and 111 EPC 1973 continue to apply. Hence, for determining whether the requirements for reimbursement of the appeal fee are met in the present case, Rule 67, first sentence, EPC 1973 is to be considered the relevant legal basis.

7.3 According to Rule 67, first sentence, EPC 1973 the appeal fee shall be reimbursed in the event of interlocutory revision or where the board of appeal deems an appeal to be allowable, if such reimbursement is ***equitable by reason of a substantial procedural violation***.

The board however finds that, even if the alleged procedural violation occurred in first-instance proceedings, it would not have been equitable to reimburse the appeal fee in the present case for the following reasons:

In the contested decision the examining division relied on document D1 to deny inventive step of the subject-matter of claim 1 of the main request then on file (see point 1.1 of the Reasons). However, the contested decision is also based on other reasons for refusing the main request then on file and contains reasons (see point 1.2 of the Reasons) why claim 1 of the main request was not clear (Article 84 EPC 1973) and why the subject-matter of that claim extended beyond the application as filed (Article 123(2) EPC). Thus, even if the inventive step objection including the appraisal of document D1 in the decision were disregarded, the contested decision would still be negative and be reasoned, and an appeal including payment of the appeal

fee would have been required in order to obtain a reversal of the first-instance decision. Hence the alleged procedural violation could not have been the immediate and only cause of the need to appeal and to pay an appeal fee.

Moreover, if the board had found that the alleged procedural violation in relation to the examining division's finding on lack of inventive step had indeed occurred, such a violation would not have been considered by the board as fundamental, justifying a reversal of the decision under appeal and a remission of the case to the department of first instance.

Thus, regardless of whether a substantial procedural violation occurred or not, the appellant, requesting that a patent be granted, had to appeal in order to obtain a reversal of the first-instance decision. Under these circumstances, a reimbursement of the appeal fee would not have been equitable in the present case and, therefore, the question whether any procedural violation was in fact committed by the examining division can be left open.

7.4 In view of the above, the request for reimbursement of the appeal fee must be refused.

Order

For these reasons it is decided that:

1. The decision under appeal is set aside.

2. The case is remitted to the first-instance department with the order to grant a patent in the following version:
   - claims 1 to 3 according to the sole request, filed with letter of 3 February 2012,
   - description pages 1 to 4, 4a, 4b, 5, 17 to 58, filed during oral proceedings of 6 March 2012,
   - drawing sheets 1/14 to 14/14, filed during oral proceedings of 6 March 2012.

3. The request for reimbursement of the appeal fee is refused.

The Registrar: The Chair:

S. Sánchez Chiquero T. Karamanli