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**Datasheet for the decision
of 1 March 2012**

Case Number: T 1849/08 - 3.4.03

Application Number: 97308267.0

Publication Number: 837508

IPC: H01L 29/739

Language of the proceedings: EN

Title of invention:

Semiconductor device and electric power conversion apparatus
therewith

Applicant:

Hitachi, Ltd.

Headword:

-

Relevant legal provisions:

-

Relevant legal provisions (EPC 1973):

EPC Art. 54, 56

Keyword:

"Novelty (no) - main and first auxiliary request"

"Inventive step (no) - second to fifth auxiliary request"

Decisions cited:

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Headnote:

Decisive for the information content of a prior art document is what a person skilled in the art reading the document would understand from it.

If to a skilled reader of a prior art document containing an isolated statement that a diagram in a figure is "not to scale", there is nothing in the figure itself or in the rest of the document supporting this statement, he would consider the statement to be made in error and disregard it.



Case Number: T 1849/08 - 3.4.03

D E C I S I O N
of the Technical Board of Appeal 3.4.03
of 1 March 2012

Appellant:
(Applicant)

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Representative:

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Decision under appeal:

Decision of the Examining Division of the
European Patent Office posted 25 April 2008
refusing European patent application
No. 97308267.0 pursuant to Article 97(2) EPC.

Composition of the Board:

Chairman: G. Eliasson
Members: R. Q. Bekkering
P. Mühlens

Summary of Facts and Submissions

I. This is an appeal against the refusal of application 97 308 267 for lack of novelty, Article 54(1) and (2) EPC 1973, (main request) over document

D1: EP 0 735 591 A,

and for lack of an inventive step, Article 56 EPC 1973 (auxiliary requests).

II. At oral proceedings before the board, the appellant applicant requested that the decision under appeal be set aside and a patent granted on the basis of the main request or on the basis of the first to fifth auxiliary requests, all filed with letter of 8 August 2008.

III. Claim 1 of the main request reads as follows:

*"A semiconductor device comprising
a semiconductor substrate having a pair of main
surfaces;
a first semiconductor region (10) of first
conductivity-type located in the substrate;
a second semiconductor region (22) of second
conductivity-type located on the first semiconductor
region;
plural third semiconductor regions (23) of second
conductivity-type having carrier density higher than
carrier density of the second semiconductor region (22);
a fourth semiconductor region (31) of first
conductivity-type located in the third semiconductor
region;
a fifth semiconductor region (40) of second*

*conductivity-type located in the fourth semiconductor region (31);
a gate insulation film (52) formed on surfaces of the second, third, fourth and fifth semiconductor regions;
a gate electrode (3) formed on the gate insulation films;
an emitter electrode (2) contacting with low resistance to the fourth semiconductor region (31) and the fifth semiconductor region (40); and
a collector electrode (1) contacting with low resistance to the first (10) semiconductor region, characterised in that the sheet carrier density of the third semiconductor region (23) is $1 \times 10^{12} \text{ cm}^{-2}$ or less."*

IV. Claim 1 of the first auxiliary request reads as follows:

*"A semiconductor device comprising:
a semiconductor substrate having a pair of main surfaces;
a first semiconductor region (10) of a first conductivity-type located in the substrate;
a second semiconductor region (22) of a second conductivity-type located on the first semiconductor region;
plural third semiconductor regions (23) of the second conductivity-type having a carrier density higher than a carrier density of the second semiconductor region (22);
a fourth semiconductor region (31) of the first conductivity-type located in the third semiconductor region;
a fifth semiconductor region (40) of the second*

conductivity-type located in the fourth semiconductor region (31);
a gate insulation film (52) formed on surfaces of the second, third, fourth and fifth semiconductor regions;
a gate electrode (3) formed on the gate insulation films;
an emitter electrode (2) contacting with low resistance to the fourth semiconductor region (31) and the fifth semiconductor region (40); and
a collector electrode (1) contacting with low resistance to the first (10) semiconductor region, characterised in that:
each third semiconductor region (23) has a thickness t within which its carrier density n is greater than a predetermined value and its sheet carrier density n_s is $1 \times 10^{12} \text{ cm}^{-2}$ or less, wherein $n_s = \int n dt$."

V. Claim 1 of the second auxiliary request reads as follows:

"An insulation gate type bipolar transistor (IGBT) (100) comprising:
a semiconductor substrate having a pair of main surfaces;
a first semiconductor region (10) of a first conductive-type [sic] located in the substrate;
a second semiconductor region (22) of a second conductive-type located on the first semiconductor region (10);
plural third semiconductor regions (23) of the second conductive-type having a higher carrier density than the carrier density of the second semiconductor region (22);

a fourth semiconductor region (30) of the first conductive-type located in each third semiconductor region (23);
a fifth semiconductor region (40) of the second conductive-type located in each fourth semiconductor region (30);
a gate insulation film (50) formed on surfaces of the second, third, fourth and fifth semiconductor regions;
a gate electrode (3) formed on the gate insulation film (50);
an emitter electrode (2) contacting with low resistance the fourth and fifth semiconductor regions;
and
a collector electrode (1) contacting with low resistance the first semiconductor region (10), wherein a sheet carrier density of each third semiconductor region (23) is $1 \times 10^{12} \text{ cm}^{-2}$ or less and a sum of a sheet carrier density of the second semiconductor region (22) and the sheet carrier density of the third semiconductor regions (23) is $1.5 \times 10^{12} \text{ cm}^{-2}$ or less."

VI. Claim 1 of the third auxiliary request corresponds to claim 1 of the first auxiliary request, however, with the characterising portion reading as follows:

"characterised in that the sheet carrier density of the third semiconductor region (23) is $1 \times 10^{12} \text{ cm}^{-2}$ or less, and the peak of its carrier density per unit volume is $2.5 \times 10^{15} \text{ cm}^{-3}$ or higher, whereby in use the third semiconductor region (23) is wholly depleted by a backward bias at a junction between the third and fourth semiconductor regions."

VII. Claim 1 of the fourth auxiliary request corresponds to claim 1 of the second auxiliary request, with the following addition:

"the volume carrier density of the second semiconductor region (22) is $7.5 \times 10^{16} / V_b \text{ cm}^{-3}$ or less and the thickness of the second semiconductor region (22) is $V_b / 12 \text{ } \mu\text{m}$ or more, where the withstand voltage of the IGBT (100) is $V_b \text{ V}$ ".

VIII. Claim 1 of the fifth auxiliary request corresponds to claim 1 of the fourth auxiliary request with the following addition:

"and wherein each third semiconductor region (23) includes a partial region (231) at which avalanche breakdown occurs more easily than the rest of that third semiconductor region (23), the partial region (231) being located below a low resistance contact point of the emitter electrode (2)."

IX. Reference is made to the following further documents:

D6: EP 0 615 292 A

D13: JP 3 205 832 A and corresponding Patent Abstracts of Japan

D14: S. M. Sze, "Physics of Semiconductor Devices", second edition, John Wiley & Sons, 1981, pages 193 to 195

- X. The appellant in substance provided the following arguments:

In document D1, the diagram depicted in figure 2 was stated to be "*not to scale*". Accordingly, the diagram only provided an indication of the relative dopant concentrations of the various regions of the structure, but no information could be derived from the diagram on any concrete dopant value or thickness of any of the regions. Accordingly, the sheet carrier density of the third semiconductor region as defined in claim 1 could not be derived from the diagram. As document D1 did not disclose any value for the sheet carrier density of the third semiconductor region anywhere else in the document, this feature was not disclosed in D1 and, therefore, the subject-matter of claim 1 was new over D1. The auxiliary requests provided the selection of additional parameters and measures, which involved the exercise of inventive skills.

Reasons for the Decision

1. The appeal is admissible.
2. *Main request*
 - 2.1 *Novelty*
 - 2.1.1 *Document D1*

Document D1 discloses an Insulated Gate Bipolar Transistor (IGBT) wherein the body regions are enclosed within respective enhancement regions of the same

conductivity type as the (underlying) lightly doped drain regions, but more heavily doped (cf figures 1 and 2 with corresponding description).

In particular, D1 discloses, in the terms of claim 1 of the appellant's main request, a semiconductor device comprising:

a semiconductor substrate having a pair of main surfaces;

a first semiconductor region (2) of first conductivity-type (eg p-type) (cf page 3, lines 16 to 18) located in the substrate;

a second semiconductor region (1) of second conductivity-type (n-type) located on the first semiconductor region;

plural third semiconductor regions (12) of second conductivity-type (n-type) having carrier density higher than carrier density of the second semiconductor region (cf page 3, lines 23 to 28; figures 1 and 2);

a fourth semiconductor region (4, 5) of first conductivity-type (p-type) located in the third semiconductor region;

a fifth semiconductor region (6) of second conductivity-type (n-type) located in the fourth semiconductor region (4);

a gate insulation film (8) formed on surfaces of the second, third, fourth and fifth semiconductor regions;

a gate electrode (7) formed on the gate insulation films;

an emitter electrode (10) contacting with low resistance to the fourth semiconductor region (4) and the fifth semiconductor region (6); and

a collector electrode (11) contacting with low resistance to the first (2) semiconductor region.

- 2.1.2 Contested by the appellant is whether in D1 the third semiconductor region (12) has a sheet carrier density of $1 \times 10^{12} \text{ cm}^{-2}$ or less.

According to D1 "*Figure 2 is a diagram (not to scale), showing the doping concentration profiles (expressed in log. atoms (at) per cubic centimeter) of the various doped semiconductor regions of the structure of Figure 1, as a function of the distance x from the semiconductor surface*" (page 3, lines 24 to 26).

The appellant argued that since the figure 2 diagram was stated to be "*not to scale*", the diagram only provided an indication of the relative dopant concentrations of the various regions of the structure, but no information could be derived from the diagram on any concrete dopant value or thickness of any of the regions. Accordingly, the sheet carrier density of the third semiconductor region (12) as defined in claim 1 could not be derived from the diagram. As document D1 did not disclose any value for the sheet carrier density of the third semiconductor region (12) anywhere else in the document, this feature was not disclosed in D1 and therefore the subject-matter of claim 1 was new over D1.

- 2.1.3 Decisive for the information content of a prior art document is what a person skilled in the art reading the document would understand from it.

Although in the passage of the description of D1 referred to above by the appellant the diagram of figure 2 is indicated to be "not to scale", the diagram is actually provided with a scale both on the horizontal and the vertical axis, providing, as stated in the description, the doping concentration profiles expressed in atoms/cm³ in logarithmic scale of the various doped semiconductor regions of the structure of figure 1, as a function of the distance x from the semiconductor surface in microns (cf page 3, lines 24 to 26). The vertical axis of the diagram of figure 2 is as a matter of fact provided with the decades of the logarithmic scale, whereby the indicated scale is also clearly consistent with the plotted value of $2 \cdot 10^{14} \text{ cm}^{-2}$ corresponding to the dopant concentration of the semiconductor layer 1 provided in the description (cf page 3, lines 45 to 48). Hence, to a person skilled in the art the diagram of figure 2 is to scale.

The description also at no other point provides any indication that, or indeed in which respect, the diagram of figure 2 would in fact not be to scale. According to the only other, formal, explicit reference to the nature of figure 2 in D1, "*Figure 2 is a diagram showing the doping concentration profiles of some doped semiconductor regions of the structure of Figure 1*" (page 2, lines 58 to 59), no mention being made of the diagram not being to scale.

In summary, there is nothing to a person skilled in the art in figure 2 itself or in the rest of document D1 supporting the above isolated statement in brackets that the diagram of figure 2 would be "not to scale".

The skilled reader would, thus, consider this statement to be made in error and disregard it.

Accordingly, in the board's judgement the skilled reader would understand figure 2 of D1 to show the doping concentration in atoms/cm³ in logarithmic scale, with the decades being indicated on the vertical axis, as a function of the distance from the semiconductor surface in microns.

- 2.1.4 As region 1 has a dopant concentration of $2 \cdot 10^{14}$ atoms/cm³, it is shown in figure 2 that region 12 has a dopant concentration of less than about $4 \cdot 10^{15}$ atoms/cm³ and a thickness of about 1.3 μm . This yields a sheet carrier density of less than $5.2 \cdot 10^{11} \text{ cm}^{-2}$ for region 12. This falls well within the claimed range of $1 \times 10^{12} \text{ cm}^{-2}$ or less.

Furthermore, factors, addressed in the decision under appeal (cf reasons, page 6), such as the assumption of thermal activation of all dopants, the box profile approximation using the highest dopant concentration of region 12 as shown in figure 2, and neglecting any dopant compensation by p-type dopants present in region 12 (see figure 2), all result in the above indicated value of $5.2 \cdot 10^{11} \text{ cm}^{-2}$ being an overestimation of the actual sheet carrier density of region 12.

Accordingly, the subject-matter of claim 1 according to the main request is not new over document D1 (Article 54(1) and (2) EPC 1973).

Therefore, the appellant's main request is not allowable.

3. *First auxiliary request*

3.1 Claim 1 according to the first auxiliary request essentially differs from claim 1 of the main request in that it specifies the following:

"each third semiconductor region (23) has a thickness t within which its carrier density n is greater than a predetermined value and its sheet carrier density n_s is $1 \times 10^{12} \text{ cm}^{-2}$ or less, wherein $n_s = \int n dt$ "

3.2 In the above calculation of the sheet carrier concentration for the main request a box profile approximation based on the highest dopant concentration of region 12 as shown in figure 2 has been used. This yields a sheet carrier density well within the claimed range. As this actually provides an overestimation of the sheet carrier density, a sheet carrier density within the claimed range is all the more obtained using the integral as specified in claim 1 of the first auxiliary request.

Accordingly, the subject-matter of claim 1 of the first auxiliary request also lacks novelty over D1 (Article 54(1) and (2) EPC 1973).

Thus, the appellant's first auxiliary request is also not allowable.

4. *Second auxiliary request*

4.1 Claim 1 according to the second auxiliary request essentially differs from claim 1 of the main request in that it contains the following addition:

"and a sum of a sheet carrier density of the second semiconductor region (22) and the sheet carrier density of the third semiconductor regions (23) is $1.5 \times 10^{12} \text{ cm}^{-2}$ or less."

4.2 According to the application, *"it is preferable that the sum of the sheet carrier density of the n layer 23 and the sheet carrier density of the n- layer 22 is made to be $1.5 \times 10^{12} \text{ cm}^{-2}$ or less in order to establish certainly enough withstand voltage in the semiconductor device of this embodiment. This makes possible to make the n layer 23 depleted when the backward bias is applied and to make the depleted layer widely and deeply enough in the n-layer and reduce the localized concentration of the electric field"* (page 16, line 20 to page 17, line 3).

As held in the decision under appeal, the objective problem to be solved relative to D1 may thus be seen as implementing the IGBT of D1 with a desired breakdown voltage.

The skilled person knows from common general knowledge that the breakdown voltage of the reverse biased junction between the fourth semiconductor region and the second with the third semiconductor region depends on the width of the depletion layer, which in turn

depends on the respective doping concentrations (cf eg document D14, page 194).

The skilled person would accordingly select the respective dopant concentrations such that the depletion layer has a sufficient width, extending through the third semiconductor region and sufficiently into the second semiconductor region, thereby arriving at dopant concentrations as claimed. No inventive skills are required to perform such routine adjustment.

Accordingly, the subject-matter of claim 1 of the second auxiliary request is obvious to a person skilled in the art and, thus, lacks an inventive step in the sense of Article 56 EPC 1973.

Therefore, the appellant's second auxiliary request is not allowable either.

5. *Third auxiliary request*

5.1 Claim 1 of the third auxiliary request corresponds to claim 1 of the first auxiliary request, however, with the characterising portion reading as follows:

"characterised in that the sheet carrier density of the third semiconductor region (23) is $1 \times 10^{12} \text{ cm}^{-2}$ or less, and the peak of its carrier density per unit volume is $2.5 \times 10^{15} \text{ cm}^{-3}$ or higher, whereby in use the third semiconductor region (23) is wholly depleted by a backward bias at a junction between the third and fourth semiconductor regions."

5.2 As discussed above with respect to the main request, in document D1 the sheet carrier density of the third semiconductor region (12) is $1 \times 10^{12} \text{ cm}^{-2}$ or less. Moreover, as can be seen from figure 2 of D1, the peak of the third semiconductor region carrier density per unit volume is $2.5 \times 10^{15} \text{ cm}^{-3}$ or higher, so that also this feature is known from D1.

Moreover, in operation of the device known from D1, ie where the junction between the third and the fourth semiconductor regions is reversed biased, it would be obvious, in order to have a depletion layer of sufficient width, to have a fully depleted third semiconductor region such that the depletion region further extends into the second semiconductor region, as discussed above.

Accordingly, the subject-matter of claim 1 of the third auxiliary request is obvious to a person skilled in the art and, thus, lacks an inventive step in the sense of Article 56 EPC 1973.

The appellant's third auxiliary request is, therefore, not allowable either.

6. *Fourth auxiliary request*

6.1 Claim 1 of the fourth auxiliary request corresponds to claim 1 of the second auxiliary request, with the following addition:

"the volume carrier density of the second semiconductor region (22) is $7.5 \times 10^{16} / V_b \text{ cm}^{-3}$ or less and the thickness of the second semiconductor region (22) is $V_b / 12 \text{ } \mu\text{m}$ or

more, where the withstand voltage of the IGBT (100) is $V_b V$ ".

- 6.2 The routine adjustments discussed above would also lead to a volume carrier density and thickness of the second semiconductor region meeting the additional criteria provided in claim 1 of the fourth auxiliary request. In particular, it would be obvious to a person skilled in the art that the second semiconductor region should be sufficiently thick so as to avoid the depletion region to reach through this layer and cause punch-through, effectively shorting the junction (cf also document D14, page 194).

Accordingly, the subject-matter of claim 1 of the fourth auxiliary request is also obvious to a person skilled in the art and, thus, lacks an inventive step (Article 56 EPC 1973).

The appellant's fourth auxiliary request is, therefore, not allowable either.

7. *Fifth auxiliary request*

- 7.1 Claim 1 of the fifth auxiliary request corresponds to claim 1 of the fourth auxiliary request with the following addition:

"wherein each third semiconductor region (23) includes a partial region (231) at which avalanche breakdown occurs more easily than the rest of that third semiconductor region (23), the partial region (231) being located below a low resistance contact point of the emitter electrode (2)."

7.2 According to the application, *"In the conventional IGBT shown in FIG. 12, the electric field concentrates at the peripheral part of the p layer 31 having a large curvature and the avalanche breakdown in the junction arises, and the avalanche current passes the p layer crossing below the n+ layer 40. Then, the voltage drop occurs due to the parasitic resistance below the n+ layer 40, and when the voltage drop gets to be over about 0.7V equivalent to the built-in potential of the pn junction, the thyristor composed of the p layer 10, the n buffer layer, the n- layer 22, n layer 23, the p layer 31 and the n+ layer 40 is turned on. This operation is called "latch up" and determines the upper bound of the safe operation region. By forming the region 231 shown in the embodiment of FIG. 11, the avalanche breakdown occurs inside the n+ layer 40 among the bottom parts of the p layer 31, that is, below the low-resistance contact part of the emitter electrode. Most of the avalanche current does not travel below the p+ layer 40 but passes the p layer 31, and the voltage drop due to the parasitic resistance below the n+ layer 40 decreases and the latch up can be avoided. Consequently, the safe operation region of the semiconductor device 102 shown in FIG.11 can be established to be wide enough and its reliability can be attained to be high enough"* (page 21, line 23 to page 22, line 19).

As held in the decision under appeal, the objective problem to be solved relative to D1 may thus be seen as providing an improved safe operation region.

Document D13 addresses this problem for a vertical power MOSFET. In particular, in D13 the parasitic bipolar transistor formed by regions 5, 4 and 1 and 2 may cause latch-up. In order to prevent this parasitic transistor from switching on, a heavily doped layer 7 of the same conductivity type as the substrate 1 is provided such that the breakdown current "*flows through a path that does not permit the parasitic bipolar diode to operate*" (cf abstract).

In view of the generally known similarities between the devices of documents D1 and D13 (see also eg document D6, column 1, line 1 to column 3, line 45; figure 9), and in particular in view of the fact that latch-up in IGBT's such as shown in D1 is caused by switching-on of the same parasitic bipolar transistor formed by regions 6, 4 and 1 with 12 in D1, it would be obvious to a person skilled in the art that the measure taken in D13 would be equally effective in the device of D1.

- 7.3 The appellant essentially argued that the main effect taught by document D13, increased breakdown voltage, was already achieved in document D1 through the provision of the enhancement region. Moreover, the actual teaching of document D1 was that the enhancement region had a higher dopant concentration than the drain layer. No information about the thickness of the extra layer was given. Accordingly, there was no motivation or reason in the prior art for the extra layer to have a sheet carrier concentration value as specified in claim 1.

However, as discussed above, the effect addressed in D13 is the prevention of latch-up, which has to be

distinguished from the effects addressed in D1 of reducing the on-voltage and increasing the breakdown voltage of the device. In case latch-up does constitute a problem in the device of D1, the skilled person would look elsewhere for a solution to this further problem and in particular consider document D13 which addresses this very issue. Moreover, the solution provided in D13 is the provision of a region which is more heavily doped than the drain region at the junction where avalanche breakdown occurs, eventually leading to latch-up of the device. Application of the solution suggested in D13 to the device of D1 would result in the provision of a region at the junction of the fourth and the third semiconductor regions with a dopant concentration above that of the third semiconductor region, causing the avalanche breakdown current to flow below a low resistance contact point of the emitter electrode of the device through a path which prevents latch-up from occurring. At the same time, however, the skilled person would be aware, based on his common general knowledge as discussed above, that a high dopant concentration of this region would reduce the width of the depletion layer at this point of the junction, thereby reducing the overall breakdown voltage of the device. Accordingly, the skilled person would not consider high sheet carrier concentrations for the partial region in the third semiconductor region lying outside the claimed range.

Accordingly, the subject-matter of claim 1 of the fifth auxiliary request is also obvious to a person skilled in the art and, thus, lacks an inventive step in the sense of Article 56 EPC 1973.

The appellant's fifth auxiliary request is, therefore, not allowable either.

Order

For these reasons it is decided that:

The appeal is dismissed.

Registrar:

Chair:

S. Sánchez Chiquero

G. Eliasson