Internal distribution code:
(A) [ ] Publication in OJ
(B) [ ] To Chairmen and Members
(C) [ ] To Chairmen
(D) [X] No distribution

Datasheet for the decision
of 19 July 2012

Case Number: T 1834/08 - 3.5.06

Application Number: 00972087.1

Publication Number: 1226507

IPC: G06F 13/42

Language of the proceedings: EN

Title of invention:
Bus System Optimization

Patentee:
Rambus Inc.

Opponent:
MICRON EUROPE Ltd

Headword:
Bus Signal Calibration/RAMBUS

Relevant legal provisions:
EPC Art. 123(2)

Relevant legal provisions (EPC 1973):
EPC Art. 56

Keyword:
"added subject matter (yes) - main request and auxiliary
requests I-V and VII"
"inventive step (no) - auxiliary request VI"

C8007.D
EPA Form 3030   This datasheet is not part of the Decision.
                       It can be changed at any time and without notice.

**Europäisches
Patentamt**

**European
Patent Office**

**Office européen
des brevets**

Beschwerdekammern

Boards of Appeal

Chambres de recours

Case Number: T 1834/08 **-** 3.5.06

D E C I S I O N
of the Technical Board of Appeal 3.5.06
of 19 July 2012

Appellant: (Opponent)	MICRON EUROPE Ltd Micron House Wellington Business Park Dukes Ride Crowthorne Berkshire RG45 6LS
Representative:	Tunstall, Christopher Stephen Carpmaels & Ransford One Southampton Row London WC1B 5HA (GB)
Respondent: (Patent Proprietor)	Rambus Inc. 1050 Enterprise Way, Suite 700 Sunnyvale, CA 94089 (US)
Representative:	Eisenführ, Speiser & Partner Johannes-Brahms—Platz 1 D-20355 Hamburg (DE)
Decision under appeal:	**Decision of the Opposition Division of the European Patent Office posted 9 July 2008 rejecting the opposition filed against European patent No. 1226507 pursuant to Article 101(2) EPC.**

Composition of the Board:

Chairman: D. H. Rees
Members: M. Müller
                  W. Sekretaruk

C8007.D

Summary of Facts and Submissions

I.   This appeal lies against the decision of the opposition
      division posted on 9 July 2008 to reject the opposition
      against European patent no. 1226507.

II.   The opponent filed a notice of appeal by telefax on
      19 September 2008, the appeal fee being paid on the same
      day. A statement of grounds of appeal was received on
      19 November 2008.

III. In the grounds of appeal, the appellant (opponent)
      refers *inter alia* to the following documents.

      OD1:   US 5 254 883 A

      OD2:   WO 99/19876

      OD3:   WO 99/03106

      OD4:   US 5 666 078 A

      OD5:   US 5 457 407 A

      Documents OD4 and OD5 had not been admitted into the
      procedure by the opposition division pursuant to
      Article 114(2) EPC 1973. The appellant challenged that
      decision and argued that they should be have been ad-
      mitted. It also argued that the decision was contradic-
      tory in its arguments.

      The appellant argued that the subject matter of granted
      claims 1 and 7 went beyond the application as originally
      filed, Article 100(c) EPC 1973, and was not disclosed in
      a manner sufficiently clear and complete for it to be
      carried out by a person skilled in the art,
      Article 100(b) EPC 1973.

The appellant argued that claim 1 lacked novelty over OD1 and inventive step over OD1 in combination with any of OD4, OD5 or common knowledge, and that claim 7 lacked an inventive step over OD2 in view of common knowledge or over OD3 in combination with OD2, Article 100(a) EPC 1973.

IV.   In response to the grounds of appeal, with letter dated 6 April 2009, the respondent (proprietor) rejected each of these objections and requested that the appeal be dismissed or that, alternatively, the patent be maintained in amended form based on one of five sets of claims filed as auxiliary requests I to V.

V.   With a summons to oral proceedings, the board expressed the following preliminary opinion: The opposition division had exercised its discretion properly when deciding not to admit D4 and D5 into the proceedings, and the decision was sufficiently reasoned in this respect. Claim 7 as granted went beyond the contents of the application documents as originally filed, while claim 1 as granted did not. Claim 1 as granted was sufficiently disclosed for it to be carried out by the person skilled in the art but lacked an inventive step over OD1.

VI.   In response to the summons, with letter dated 18 June 2012, the respondent filed two additional sets of claims as further auxiliary requests VI and VII.

VII.   Claims 1 and 7 as granted read as follows:

        "1. A method of determining a compensating driver current offset for a slave device (12a) transmitting

data to a master device (11) via a data bus (30), the
method comprising:

driving data onto the data bus (30) at the slave device
(12a);

receiving the data at the master device (11) in a
comparator circuit;

comparing a voltage level of the data to a reference
voltage;

generating a signal based on the comparison between the
reference voltage and the voltage level of the data,
wherein the signal is representative of a direction to
adjust the voltage level of the data such that the
voltage level of the data is adjusted toward the
reference voltage;

communicating the signal from the master device (11) to
the slave device (12a); and

adjusting a value in a register (321, 331) in accordance
with the signal, wherein the register (321, 331) is in
the slave device (12a) and the value in the register
(321, 331) defines a driver current offset for the slave
device (12a).

7. A method of operation in a system that includes a
first integrated circuit device (11, 12a) to the second
integrated circuit device (12a, 11), the method
comprising:

transmitting a data sequence from the first integrated
circuit device (11, 12a) to the second integrated
circuit device (12a, 11);

sampling the data sequence by the second integrated
circuit device (12a, 11) to produce receiver data;

transmitting the receiver data from the second
integrated circuit device (12a, 11) to the first
integrated circuit device (11, 12a);

performing a comparison between the data sequence and
the receiver data; and
based on the comparison, generating information
representative of a calibrated timing offset; and
using the information representative of the calibrated
timing offset to adjust timing associated with
transferring data from the first integrated circuit
device (11, 12a) to the second integrated circuit device
(12a, 11)."

VIII. In auxiliary requests I, II and VI, claim 1 is identical
to claim 1 of the main request, in auxiliary requests
III-V claim 1 and its dependent claims 2-5 have been
deleted, and in auxiliary request VII claim 1 has been
limited by addition of the following features at the end:

"... characterized in that driving data onto the bus (30)
further comprises driving a high data value on a first
signal line (335a) of the data bus (30) and driving a
low data value on a second signal (335b) line of the
data bus (30); and generating the voltage of the data
from an intermediate voltage level of the high data
value and low data value."

IX.   Claim 1 of auxiliary request III and claim 5 of auxilia-
ry request VII are identical to claim 7 of the main
request. Claim 7 of auxiliary request I and claim 1 of
auxiliary request IV are identical to claim 7 of the
main request except for the addition of the following
feature at the end:

"... wherein the timing offset is determined upon
detection of a threshold number of bit errors."

Claim 7 of auxiliary request II and claim 1 of auxiliary request V are identical to claim 7 of the main request except for the addition of the following feature at the end:

"... wherein the data sequence has a balanced number of 0-1 and 1-0 transitions, and wherein the second integrated circuit device (12a) operates as a phase detector."

In auxiliary request VI, claim 7 is identical to claim 7 of the main request except for the following addition at the end:

"... characterized in that transmitting the data sequence from the first integrated circuit device (11, 12a) to the second integrating circuit device (12a, 11) includes transmitting a calibration clock signal that is shifted by about 90° with respect to the main clock signal; and
transmitting data from the first integrated circuit device (11, 12a) to the second integrated circuit device (12a, 11) includes transmitting data in conjunction with transmitting the main clock signal."

X.   At the end of the oral proceedings, the chairman announced the decision of the board.

Reasons for the Decision

1.   The appeal is admissible (see in particular points I and II above).

Admission of OD4 and OD5

2.   In view of the outcome of the appeal the question whe-
        ther OD4 and OD5 should have been or should be admitted
        is moot.

Admission of auxiliary requests VI and VII

3.   Independent claims 7 and 18 of auxiliary request VI have
        been amended - over claims 7 and 19 as granted - by in-
        corporating the features of claim 16 as granted, in par-
        ticular a 90° clock shift. Independent claim 1 of auxil-
        iary request VII has been amended over claim 1 as gran-
        ted to incorporate the features of claims 2 and 3 as
        granted. Except for discarding the now redundant claims
        and renumbering the remaining ones, no further amend-
        ments have been made.

4.   The filing of auxiliary requests VI and VII constitutes
        an amendment of the respondent's case which the board
        has discretion to admit under Article 13 (1) RPBA. Since
        both amendments are based on dependent claims as granted
        and are not particularly complex, and since therefore
        both the board and the appellant should be expected to
        deal with these requests without undue effort or delay
        during the oral proceedings, the board exercised its
        discretion to admit both requests.

Contradictions in the decision

5.   The appellant argues that the decision contains contra-
        dictions that would "make it, as a whole, irrational (in
        the legal sense) and incomprehensible" (grounds of
        appeal, point 2.2). Specifically, the decision is alle-

C8007.D

gedly contradictory in its interpretation of "signal ...
representative of direction" (grounds of appeal, point 3
ff.) While the appellant does not explicitly refer to
any specific legal requirement, the board takes it that
the appellant considers the decision therefore to be
insufficiently reasoned in the sense of Rule 111(2) EPC.

5.1. The decision explicitly states the conclusions (see p. 3,
esp. the last par.) that the original term "up/down sig-
nal" and the new term "signal ... representative of a
direction" are "synonymous in the given context" of ad-
justing the voltage level towards the reference voltage,
and that the K value of D1 is not considered to consti-
tute such a signal. In the board's judgment, the deci-
sion also provides sufficient reasons for why the oppo-
sition division deemed this to be the case (*loc. cit.*).

5.2. The board therefore does not to share the appellant's
perception that the decision is contradictory, let alone
that it is insufficiently reasoned in this respect.

The invention

6. The invention generally relates to method and apparatus
for adjusting timing and voltage characteristics of data
signals exchanged between a master and a slave device
(see application as published, p. 4, lines 2-4). In this
context, independent claims 1, 5 and 6 of the patent re-
late to voltage adjustment, while claims 7 and 19 of the
patent relate to timing adjustment. In the following,
these groups of claims will be discussed separately,
starting with claim 7 of the patent, *i.e.* claim 7 of the
main request.

Main request

Article 100(c) EPC 1973, Article 123(2) EPC, Claim 7

7.   Claim 7 of the patent as granted relates to the adjust-
       ment of the timing characteristics of data transmission
       between two integrated circuit devices (*viz.* master and
       slave). According to the claimed method, the first de-
       vice transmits a data sequence to the second device
       which samples it to produce so-called "receiver data"
       which is transmitted back. At the first device, the ori-
       ginal data sequence and the receiver data are compared
       and, based on the comparison, a calibrated timing offset
       is generated to be used for future data transmission
       between both devices.

7.1.   The description discloses essentially two techniques to
       achieve timing calibration, called respectively "90° ca-
       libration" (p. 23, line 15 - p. 24, line 8, and original
       claim 43) and "scanning window" calibration (p. 25,
       lines 8-23, and original claim 49; cf. also grounds of
       appeal, points 5.1.2-5.1.4).

       According to the 90° calibration technique, the sender
       shifts the internal transmit clock signal by 90° before
       sending the data sequence and the receiver will, depen-
       ding on the phase difference between them, receive the
       sent data correctly, or will receive a "0" as a "1" or
       vice versa (cf. *e.g.* description, p. 24, lines 2-8). De-
       pending on this result, the master will increment or de-
       crement the read/write offset value until a centering
       offset value has been obtained (p. 24, lines 16-18). It
       is disclosed that the technique is symmetric in that
       sender and receiver can be master and slave, respective-

ly, or vice versa (p. 23, lines 20-22, and p. 24, lines
25-27).

According to the scanning window technique, a range of
offset values is "scrolled through": That is, each of a
range of offsets is applied to the read/write clock so
that the clock transition moves in relation to the data
eye. For each of these offsets the master will try to
detect a 0-to-1 or 1-to-0 transition in order to locate
the leading edge of the data eye at one offset value and
the lagging edge at another one (cf. p. 25, lines 13-16).
The centering offset is obtained as by averaging these
offset values.

7.2.   The appellant argues that claim 7 was broadened over the
       original disclosure "to such an extent that it no longer
       contains any of the essential integers of the original
       disclosed embodiments" (see grounds of appeal, point
       5.1.6). In particular, as the appellant expressed during
       oral proceedings, both embodiments relied on some kind
       of clock shifting during the testing phase, in a single
       90° shift or in a number of phase shifts, whereas claim
       7 only requires a clock adjustment only as final timing
       adjustment, *i.e.* after the testing. This omission from
       claim 7 amounted to an impermissible generalisation of
       the disclosed invention. In the grounds of appeal (*loc.
       cit.*) more essential features were mentioned which claim
       7 had to contain, in the appellant's view, in order to
       conform with Article 123 (2) EPC. With the summons to
       oral proceedings (see point 11 ff.), the board also
       raised the following issue: According to the respondent,
       claim 7 as granted was based on original claim 43 in
       combination with the description on pages 23 and 24 (see
       submission dated 6 April 2009, feature table on p. 17).

Original claim 43 contained the feature of "shifting the transmit clock in the master by 90°" and the description on pages 23 and 24 appeared to relate to the 90° calibration. In particular, the features of claim 7 relating to "data sequences" being transmitted, received and compared appeared not to appear to be disclosed in relation to the "scanning window" technique.

7.3.   The respondent explained that the description disclosed three techniques for timing calibration, counting as two the alternatives of the 90° calibration (p. 23, line 15 - p. 24, line 24; vs. p. 24, line 25 - p. 25, line 1), of which only the first one was fully developed, whereas the others were disclosed in lesser detail. The skilled person would however understand that missing details from the scanning window technique had to be adapted from the detailed disclosure of the 90° calibration. In particular, the respondent referred to the description on page 26 (lines 6-7) which mentions that the "scanning window feedback mechanism is applied to voltages instead of timing", argued that the skilled person would understand this to refer to the 90° calibration technique, too, and suggested that the skilled person would take the term "feedback mechanism" to refer to the transmission, sampling, retransmission and comparison of data sequences according to the 90° calibration technique as disclosed on pages 24-25. Furthermore, the respondent, while conceding that original claim 43 covered the 90° calibration only, pointed out that original claim 49 covered the scanning window calibration and, as such, did not require a 90° clock shift: Claim 7 as granted was drafted to cover both embodiments so that the omission of the 90° clock shift feature was justified.

7.4. The board notes that the application as originally filed refers to, in the context of the 90° calibration, the transmission of a data sequence, a data pattern or a large block of data comprising several bits (p. 23, lines 22 and 30-31 and p. 24, line 13-14; claim 43) and its sampling into "receiver data", retransmission to the sending device, and comparison in order to detect a phase offset (p. 23, line 30 - p. 24, line 8; claim 43), in each step of the iteration which, as a whole, eventually produces the centering offset (p. 24, lines 16-18). In contrast, the description of scanning window calibration refers only to individual 0-to-1 or 1-to-0 transitions and neither to a transmission nor to the comparison of a data sequence as part of one iteration step. The board concedes that, as the respondent points out (submission of 18 June 2012), some data must be transmitted from the sender (*e.g.* the master) to the receiver (*e.g.* the slave) and back also in the scanning window approach. This does not imply, however, that a data sequence is transmitted in each iteration step. The board is also unable to accept that the skilled person would understand the mention of the "scanning window feedback mechanism" on page 26 (lines 6-7) as a reference to the transmit-sample-retransmit cycle disclosed as part of the 90° calibration technique disclosed on page 24.

7.5. The board therefore concludes that claim 7 of the patent as granted does not subsume the scanning window embodiment but is only supported by the 90° calibration embodiment. For the same reason, the board dismisses original claim 49 as a possible basis for claim 7 as granted.

7.6. In the context of the 90° calibration embodiment however the board is not aware of any statement in the applica-

tion which would justify the omission of the clock shif-
ting feature. According to the description (p. 25, lines
2-7), the circuits in figures 25-27 require circuits
"providing the 0° and 90° shifted clock signals" in the
master - where they are "easily available in many DLL/
PLL designs" and there is no disclosure to the effect
that these circuits could be dispensed with. However
their omission in the granted claims would be understood
by the skilled reader to mean just that.

7.7.   The board therefore concludes that claim 7 as granted
        extends beyond the application as originally filed, and
        that so does claim 19.

7.8.   For this reason alone, the decision under appeal must be
        set aside.

Auxiliary requests I-V and VII

8.   Since claim 7 of auxiliary requests I and II, claim 1 of
        auxiliary requests III-V and claim 5 of auxiliary
        request VII share the deficiency of claim 7 of the main
        request under Article 123 (2) EPC, auxiliary requests I-
        V and VII are not allowable for the same reason as the
        main request.

Auxiliary request VI

Article 100(b,c) and 83 EPC 1973, Article 123(2) EPC

9.   The appellant argues (see grounds of appeal, point 4.1
        ff.) that the replacement in claim 1 of the original
        term "up/down signal" by the new term "signal ... repre-
        sent of a direction" goes beyond the application as ori-
        ginally filed and that the decision is wrong in finding

C8007.D

that it does not. The appellant further objects that,
due to the replacement, amended claims 1-6 as granted
are insufficiently disclosed because they are "fundamen-
tally broader than the embodiments described in the de-
scription" (grounds of appeal, point 4.1.8). The res-
pondent considers, in agreement with the decision, that
the two expressions are synonymous in the given context.

9.1.   The appellant argues that the patent would encompass two
       things that were not originally envisaged (see grounds
       of appeal, point 4.1.7) by stating that a signal ...
       representative of direction

       a)   "envisages far more complex arrangements than a
             simple up/down signal could ever have achieved",
             for example the use of "binary search algorithms"
             in addition to "simple linear searches" towards the
             reference voltage, and

       b)   covers the use of an "up/stop" or "down/stop" sig-
             nal in addition to an "up/down signal".

9.2.   During oral proceedings the appellant reiterated the ob-
       jection according to which the term "signal ... repre-
       sentative of a direction" is more general than the term
       "up/down signal" but otherwise merely referred to its
       submissions in writing. The following argument is thus
       based on the board's preliminary opinion sent with the
       summons.

9.3.   As regards a) the board considers that neither present
       claim 1 nor original claim 41 specify or imply what vol-
       tage level the calibration process has to start from nor
       how the "signal ... representative of direction" or the

"up/down signal" are to be used, respectively, for ad-
justing the voltage level towards the reference voltage,
i.e. in what kinds of search algorithms. Thus the two
expressions are equivalent in the "complex[ity of the]
arrangements" which they might be taken to envisage. As
regards b) the board agrees with the decision (p. 3,
last par.) in considering that an "up/stop" or a "down/
stop" signal are not "representative of direction":
Rather, these signals merely represent the fact that the
voltage level should be adjusted, whereas the direction
and the amount of this adjustment are predetermined
independent of the signal.

9.4.   The board thus agrees with the decision under appeal and
        the respondent that the terms are synonymous in the
        claimed context, both defining a signal which indicates
        one of two possible directions (up or down) in which the
        reference voltage is to be adjusted but neither the ad-
        justment step nor the target value of the adjustment.

9.5.   In the board's judgement thus amended claim 1 does not
        extend beyond the application as originally filed and
        neither do, for the same reasons, claims 5 or 6. As a
        consequence of the board's position that the terms are
        synonymous, also the added matter objection to these
        claims fails.

Prior Art

10.   Document OD1, undisputedly the most relevant piece of
        prior art at hand, addresses the problem of minimizing
        variations of voltage levels and current on a data bus
        between master and slave devices (see col. 2, lines 11-
        24 and 40-47; and fig. 1). To this end, circuitry is

provided in the slave device (col. 13, lines 8 ff. and fig. 7) for adjusting the current and voltage level under the control of a so-called K value held in a dedicated register (see *e.g.* col. 13, lines 45-60 and col. 15, lines 12-15) in the slave (see col. 15, lines 10-11). OD1 further discloses a calibration process during which the master device compares the voltage level on the bus and the reference voltage and determines an "updated K value" (see *e.g.* col. 15, line 22) which is sent to the slave device to set the register value accordingly (cf. *e.g.* col. 15, line 26-27).

11.   The circuitry according to OD1 which eventually controls the voltage and current on the data transmission line (fig. 4, no. 111) has, as the respondent explains, two distinguished components, depicted respectively in figures 4 and 7.

11.1. One is the current mode driver as disclosed in figure 4 and described in col. 7 ff.). It comprises an array of transistors (no. 101), which can be selectively "turned on" to control voltage and current on the data transmission line (cf. col. 9, lines 42-55). The transistors are controlled by a binary value which is received from the output lines of a "current controller" (see nos. 120 and 103; and col. 9, line 56 - col. 10, line 7) and via NAND gates and inverters (nos. 102 and 106).

11.2. The other is the current controller itself. OD1 discloses two embodiments of the controller (figs. 6 and 7), the second of which is relevant for the case to hand. According to this embodiment, the controller provides an array of capacitors (no. 163) which can be selectively coupled to a line (no. 167) in accordance with the value

K held in register REG (cf. OD1, e.g. col. 13, lines 42-
49; and col. 14, lines 17-22). Logic circuitry (esp.
no. 157; col. 13, lines 50-68) is also provided to
"translate" the resulting voltage into a binary value
which is eventually used to control the transistor array
as just discussed (see fig. 4).

11.3. The K value, which indirectly determines voltage and
current on the data transmission line, can be set by the
user (see OD1, col. 12, lines 66-68 and col. 14,
lines 62-64). However, OD1 also discloses that the value
of K may have to be calibrated, especially in order to
compensate for manufacturing variance in the capacitance
of the capacitors (fig. 7, no. 163; col. 14, line 65 -
col. 15, line 2).

11.4. At every point during this calibration process, the vol-
tage on the data transmission line is determined by the
current value of K (col. 15, lines 12-15). The slave
whose K value is being calibrated sends a data packet to
the master (col. 15, lines 15-16) which compares the
voltage level of the received data to a reference vol-
tage (lines 16-20). Based on this comparison result,
which must be represented by some signal, the K value is
updated and sent to the slave to update the register
accordingly (lines 22-23).

11.5. OD1 discloses that K may initially be set to zero and
repeatedly increased during calibration (col. 15, lines
8-10 and 20-21). Alternatively, calibration may start
with K set to a large value which is repeatedly de-
creased (lines 32-39) or that K can be found via a "bi-
nary search ... as part of the calibration process"
(lines 29-31) in which case, as the board understands it,

K may be increased or decreased in response to the voltage comparison.

Inventive Step

12.   Claim 1 of auxiliary request VI is identical with claim 1 as granted.

13.   The respondent argues that the mentioned calibration process according to OD1 does not qualify as a "method of determining a compensating driver current offset" as required by the preamble of claim 1 and that the register REG of OD1 does not "[define] a driver current offset" as required by the last feature of claim 1. Rather, the process of OD1 has to be seen as a process of "calibrating the calibrator", as the respondent put it during oral proceedings, in a phase strictly preceding the current offset calibration as claimed. OD1 disclosed a second phase by discussing what "control logic 157" would do "during operation" (col. 15, lines 58-64).

14.   The board cannot follow this argument. First, as discussed above, control logic 157 "translates" the voltage on line 167 (fig. 7) into a binary value which, if indirectly, determines voltage and current on data transmission line 111 (fig. 4). This translation is thus an integral part of the calibration process of OD1 rather than a separate phase. Moreover, since OD1 discloses calibration of each slave individually with respect to the master (col. 15, lines 10-11), the final K value in register REG constitutes, in the board's judgement, a "driver current offset for the slave device".

15.   According to OD1, the updated K value is transmitted to
        the slave and there simply stored in the register. This
        K value is not "representative of direction" but repre-
        sents the new target value directly.

15.1.   The board thus concludes that claim 1 differs from OD1
        in that it requires the transmission of a "signal repre-
        sentative of direction to adjust the voltage level" and
        the adjustment of the corresponding register at the
        slave "in accordance with this signal".

15.2.   In the grounds of appeal (point 4.2.3), the appellant
        suggested that the objective technical problem is to
        avoid the "exchange of redundant information". In fact,
        while the entire K value consists of several bits (for
        instance five, as illustrated in figs. 4 and 7), the
        signal representative of direction could consist in as
        little as one or two bits. Therefore the board considers
        that in comparison with OD1, claim 1 solves the problem
        of reducing the amount of communication between master
        and slave.

15.3.   The board agrees with the appellant that the skilled
        person would not need to exercise an inventive step in
        order to solve this problem by transmitting only the
        comparison result and leaving it to the slave to deter-
        mine the new K value.

15.4.   In the summons, the board presented this as its prelimi-
        nary finding and invited the respondent to comment on it,
        specifically in view of the fact that the appellant's
        argument in the grounds of appeal had been brief and not
        been addressed by the respondent in its response. The
        respondent chose not to address this issue in its res-

ponse to the summons and stated during oral proceedings that it would not want to argue inventive step based on this difference.

15.5. The board thus concludes that claim 1 of auxiliary request VI lacks an inventive step over OD1, and that so do independent claims 5 and 6.

Summary

16.   There being no further requests, the patent must be revoked.

Order

For these reasons it is decided that:

1.   The decision is set aside.

2.   The patent is revoked.

The Registrar: The Chairman:

B. Atienza Vivancos   D. H. Rees