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**Datasheet for the decision
of 1 June 2012**

Case Number: T 1762/08 - 3.5.04
Application Number: 98118460.9
Publication Number: 905973
IPC: H04N5/46, H04N5/45, H04N5/44,
H04N5/907, G06T1/20
Language of the proceedings: EN

Title of invention:

Television receiver, video signal processing device, image processing method and device

Applicants:

Panasonic Corporation
Texas Instruments Incorporated

Headword:

Relevant legal provisions:

EPC Art. 123(2)

Keyword:

Extension of subject-matter - yes

Decisions cited:

G 0010/93

Catchword:



Case Number: T1762/08 - 3.5.04

D E C I S I O N
of the Technical Board of Appeal 3.5.04
of 1 June 2012

Appellants:

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Decision under appeal:

**Decision of the Examining Division of the
European Patent Office posted 8 May 2008
refusing European patent application No.
98118460.9 pursuant to Article 97(2) EPC.**

Composition of the Board:

Chairman: B. Müller
Members: R. Gerdes
M. Paci

Summary of Facts and Submissions

- I. The appeal is against the decision of the examining division to refuse European patent application No. 98 118 460.9 posted on 8 May 2008.
- II. The patent application was refused by the examining division because the subject-matter of claims 1 and 4 according to the applicants' sole request lacked an inventive step (Article 56 EPC).
- III. The appellants appealed against this decision and requested that it be set aside and that a patent be granted based on the set of claims 1 to 6 which were enclosed with the decision. As an auxiliary measure oral proceedings were requested.
- IV. In a communication annexed to the summons to oral proceedings the board *inter alia* expressed doubts as to whether the claimed subject-matter could be derived directly and unambiguously from the application as originally filed (Article 123(2) EPC). The board also raised objections under Article 84 EPC 1973 and made comments as to inventive step.
- V. By letter of 9 March 2012 the appellants withdrew the request for oral proceedings. In response the board cancelled the oral proceedings and announced that a decision would be given in writing.
- VI. Claims 1 to 3 of the sole request read as follows:

"1. An image processing device comprising:
an input section (2040) for receiving up to two sets of 16-bit digital video signals simultaneously as image data to be processed;

a digital signal processing section (2014) including input ports for receiving up to three 16-bit image data units simultaneously, a plurality of processing elements (PE_1, \dots, PE_N) allocated to respective pixels corresponding to one scanning line in a one-to-one relationship for performing a same operation in accordance with a common instruction, each processing section further including a pair of register files (RF_0, RF_1), output ports for outputting up to three 16-bit image data units simultaneously, the digital signal processing section (2014) receiving, processing, and outputting the image data for each scanning line;

an image memory (2050) having a fixed memory region and capable of performing a write operation and a read operation in parallel and independently, the image memory (2050) receiving and outputting the image data for each scanning line;

an output section (2070) for outputting up to two sets of 16-bit digital video signals simultaneously as processed image data;

data bus means (2072) for connecting the input section (2040), the digital signal processing section (2014), the image memory (2050), and the output section (2070) with one another; and

control means (2074) for controlling the input section (2040), the digital signal processing section (2014), the image memory (2050), and the output section (2070) in accordance with program data,

wherein the data bus means (2072) connects the input section (2040), the digital signal processing section (2014), the image memory (2050) and the output section (2070) via multiplexers (2082, 2084, 2086),

wherein output terminals of a first multiplexer (2082) are connected to input ports of the digital signal processing section (2014), output terminals of a second multiplexer (2084) are connected to input ports of the

image memory (2050), and output terminals of a third multiplexer (2086) are connected to input ports of the output section (2070),
wherein output ports of the input section (2040) are connected to input terminals of the first multiplexer (2082) and connected to input terminals of the second multiplexer (2084),
wherein output ports of the digital signal processing section (2014) are connected to input terminals of the second multiplexer (2084) and are connected to input terminals of the third multiplexer (2086),
wherein output ports of the image memory (2050) are connected to input terminals of the first multiplexer (2082) and to the input terminals of the third multiplexer (2086).

2. An image processing device according to claim 1, wherein the digital signal processing section (2014) includes a video signal processing device comprising:
a first converter for receiving a plurality of video data units corresponding to a plurality of pixels connected to one scanning line as an input video signal, and converting the plurality of video data units into a plurality of video data sets, each of the plurality of video data sets including at least two video data units;
an operator for processing the plurality of video data sets and outputting a plurality of processed video data sets; and
a second converter for converting the plurality of processed video data sets into a plurality of processed video data units corresponding to a plurality of pixels connected to one scanning line, and outputting the plurality of processed video data units as an output video signal.

3. An image processing device according to claim 2, wherein the operator includes a plurality of processor elements, and each of the plurality of processor elements processes at least two image data units included in each of the plurality of video data sets."

Claims 4 to 6 are of no relevance to the present decision.

VII. The appellants did not make submissions in reply to the objections, in particular those under Article 123(2) EPC, that the board had raised in the communication annexed to the summons to oral proceedings.

Reasons for the Decision

1. The appeal is admissible.
2. Although the decision under appeal is based solely on the ground of lack of inventive step, the board has the power to examine (*ex officio*) whether the application also meets other requirements of the EPC (see decision G 10/93, OJ EPO 1995, 172, Order of the decision).
3. According to Article 123(2) EPC the European patent may not be amended in such a way that it contains subject-matter which extends beyond the content of the application as filed. According to the established case law of the boards of appeal, an amendment should be regarded as introducing subject-matter which extends beyond the content of the application as filed if the overall change in the content of the application results in the skilled person being presented with information which is not directly and unambiguously derivable from the application as originally filed.

3.1 The application relates *inter alia* to an image processing device incorporating a single-instruction multiple-data (SIMD) processor for video signals such as television signals.

3.2 Claim 1 is based on independent claim 7 as originally filed together with claim 14 and figure 8 as originally filed. It relates to a particular embodiment ("Example 5") of the application illustrating a specific data bus arrangement for the image processor shown in figure 7. The arrangement is described from page 43, line 14 to page 44, line 30 of the application as originally filed.

Claim 1 specifies a flexible architecture (see figure 8) consisting of several multiplexers (2082, 2084, 2086), an input section (2040) and an output section (2070), which are arranged around an SIMD image processor (2014) and an image memory (2050). Due to the multiplexers the input ports of the image processor can be selectively connected to any of the output ports of the input section or the output ports of the image memory. Similarly, the output of the image processor can be connected to any of the input ports of the image memory or an input port of the output section. The switching of the multiplexers is controlled by a timing control unit 2074, see figure 7. Due to this configurability the SIMD image processor according to figure 8 and claim 1 can be used for a variety of applications.

3.3 The additional features of dependent claims 2 and 3 according to the current request are based on claims 29 and 30 as originally filed. Claim 29 was filed as an independent claim and relates to the embodiment

designated as "Example 6" (see page 70, line 7 to page 79, line 24 and figures 27 to 31).

Example 6 illustrates another architecture including an SIMD image processor. Figure 27 shows an SIMD image processor (3001) having its input and output ports connected to a serial-parallel converter (3016) and a parallel-serial converter (3017), respectively. The serial-parallel converter serves to convert, for example, two pixels of an input video signal, i.e. two so-called video data units, to one video data set having twice the number of bits as a video data unit. The parallel-serial converter performs the inverse operation on the video data sets that are output from the image processor. The architecture of example 6 allows the number of processor elements of the SIMD image processor to be reduced with respect to the number of effective pixels connected to one scanning line (see page 79, lines 1 to 4), the reduction being proportional to the ratio between the number of bits of a video data set and a video data unit. A SIMD image processor having a certain number of processing elements can therefore be used for the processing of video signals having different formats, i.e. a different number of pixels per horizontal scanning line.

- 3.4 The embodiments according to example 5 (relating to claim 1) and example 6 (relating to claims 2 and 3) were not presented in the application as filed such that it was directly and unambiguously derivable that they could be combined.

On the contrary, the embodiments cannot be combined without major modifications. Example 5 and claim 1 specify routing of 16-bit video data via multiplexers.

According to claim 1 the digital signal processing section, i.e. the SIMD image processor, receives three 16-bit image data units and outputs three 16-bit image data units. However, example 6 gives details of serial-parallel and parallel-serial conversion of two 8-bit video data units.

Therefore the combination of the subject-matter of claim 1 and that of either claim 2 alone or claims 2 and 3 extends beyond the content of the application as originally filed (Article 123(2) EPC).

4. Since the above finding precludes the grant of a patent, the further objections raised in the communication annexed to the summons to oral proceedings need not be dealt with in this decision.

Order

For these reasons it is decided that:

The appeal is dismissed.

The Registrar:

The Chairman:



K. Boelicke

B. Müller

Decision electronically authenticated