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**Datasheet for the decision
of 20 October 2011**

Case Number: T 1751/08 - 3.5.02

Application Number: 03022637.7

Publication Number: 1406392

IPC: H03M 13/11, H03M 13/25,
                              H04L 27/18, H04L 27/34

Language of the proceedings: EN

Title of invention:
Variable modulation with LDPC (low density parity check)
coding

Applicant:
Broadcom Corporation

Opponent:
-

Headword:
-

Relevant legal provisions:
EPC Art. 84, 123(2), 56

Keyword:
"Clarity and support by the description (yes - after
amendment)"
"Inventive step (yes)"

Decisions cited:
-

Catchword:
-

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Case Number: T 1751/08 **-** 3.5.02

D E C I S I O N
of the Technical Board of Appeal 3.5.02
of 20 October 2011

Appellant:	Broadcom Corporation
(Applicant)	5300 California Avenue
	Irvine, CA 92617 (US)

Representative:	Jehle, Volker Armin
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Decision under appeal:	**Decision of the Examining Division of the European Patent Office posted 18 April 2008 refusing European patent application No. 03022637.7 pursuant to Article 97(2) EPC.**

Composition of the Board:

Chairman:	M. Ruggiu
Members:	M. Rognoni
	R. Moufang

C6691.D

Summary of Facts and Submissions

I.   The appellant (applicant) appealed against the decision
       of the examining division refusing European patent
       application No. 03 022 637.7.

II.   In the contested decision, the examining division found,
       inter alia, that claim 1 of the main request filed at
       the oral proceedings held on 7 November 2007 lacked
       support according to Article 84 EPC.

III.   In a communication dated 25 May 2011 summoning the
       appellant to oral proceedings, the Board addressed a
       number of issues concerning the appellant's request
       filed with the statement of grounds of appeal and
       referred, *inter alia*, to the following prior art:

       D8:   B. Myhre *et al.:* "LDPC Coded Adaptive Multilevel
             Modulation for Slowly Varying Rayleigh-Fading
             Channels", Proc. of IEEE Norwegian Symposium on
             Signal Processing, pages 129 to 134, Trondheim,
             Norway, Oct. 18 - 20, 2001;

       D9:   U. Wachsmann *et al.:* "Multilevel Codes:
             Theoretical Concepts and Practical Design Rules",
             IEEE Transactions on Information Theory, Vol. 45,
             No. 5, July 1999, pages 1361 to 1391.

IV.   Oral proceedings were held before the Board on
       20 October 2011.

V.   The appellant requested that the decision under appeal
       be set aside and that a patent be granted on the basis

of the single claim of the new main request filed at
the oral proceedings.

VI.   The single claim of the appellant's request reads as
        follows:

"An encoder that performs both LDPC (Low Density Parity
Check) encoding and modulation encoding on a binary
sequence to generate an LDPC coded modulation signal,
the encoder comprising:

        an LDPC encoder that performs LDPC coding on the
binary sequence to generate an LDPC codeword that
includes a plurality of LDPC coded bits;
said LDPC coding having 64800 variable nodes, the first
4320 of said variable nodes having a degree 13, the
residual variable nodes having a degree of three or
less,

        a S/P (serial to parallel) mapping functional
block adapted to divide the LDPC codeword into 3 paths;
whereby the second n bits of the plurality of LDPC
coded bits of the LDPC codeword are provided to a first
path of the 3 paths; the last n bits of the plurality
of LDPC coded bits of the LDPC codeword are provided to
a second path of the 3 paths; and the first n bits of
the plurality of LDPC coded bits of the LDPC codeword
are provided to a third path of the 3 paths,

        wherein the LDPC coded bits of said LDPC codeword,
which are output from the three paths, are grouped
together to form one LDPC coded symbol; such that each
LDPC coded bit forms part of one of a plurality of the
LDPC coded symbols,

        wherein the bits from the first path represent the
most significant bit "MSB" of each symbol, the bits
from the second path represent the inside significant

bit "ISB" of each symbol, and the bits from the third
path represent the least significant bit "LSB" of each
symbol,

characterized by

two modulation encoders being adapted to operate
cooperatively such that each modulation encoder
receives the LDPC coded symbols according to a
predetermined cycle,

said predetermined cycle being performed as
follows:

the first 4320 symbols and the odd symbols formed
thereafter are provided to a first modulation encoder,
the even symbols after the first 4320 symbols are
provided to a second modulation encoder,

wherein each modulation encoder performs
modulation encoding on the LDPC coded symbols that it
receives thereby generating corresponding pluralities
of LDPC coded modulation symbols;

each modulation encoder being operable to perform
a different modulation, said modulations having a fixed
constellation shape but different constellation
mappings;

wherein the first modulation encoder is adapted to
perform the mapping (0) as specified in Figure 19A; and
the second modulation encoder is adapted to perform the
mapping (8) as specified in Figure 21A,

the encoder being adapted to output the code
modulation symbols from the modulation encoders as a
signal sequence to form the LDPC coded modulation
signal that is a variable modulation signal."

VII. The appellant essentially argued that the single claim
      was limited to the embodiment of the invention shown in
      Figure 22 and thus found full support in the

application as filed (Article 84 EPC). In particular, the claim now comprised a specific combination of LDPC encoding and modulation encoding based on two predetermined maps. As shown in the application, using two separate mappings for modulation encoding according to the cycle recited in the claim provided for a significant improvement in the encoder's performance.

There was no suggestion in the prior art that it could be advantageous to perform modulation encoding on an LDPC codeword by switching between a first map and a second map on a symbol by symbol basis after coding a first set of high-degree variable nodes with the first map. Just on the basis of general hints in the prior art that under certain circumstances it might be useful to change constellation and/or mapping, the skilled person would have had no incentive to develop the particular combination of LDPC encoding and modulation encoding recited in the claim.

Hence, the subject-matter of the claim involved an inventive step within the meaning of Article 56 EPC.

Reasons for the Decision

1.   The appeal is admissible.

Article 84 and Article 123(2) EPC

2.1   The claim according to the appellant's request relates essentially to an encoder that performs both LDPC (Low Density Parity Check) encoding and modulation encoding

on a binary sequence to generate an LDPC coded
modulation signal. It comprises the following features:

(a)   an LDPC encoder that performs LDPC coding on the
       binary sequence to generate an LDPC codeword that
       includes a plurality of LDPC coded bits;

(b)   said LDPC coding having 64800 variable nodes, the
       first 4320 of said variable nodes having a degree
       13, the residual variable nodes having a degree of
       three or less,

(c)   a S/P (serial to parallel) mapping functional
       block adapted to divide the LDPC codeword into 3
       paths; whereby the second n bits of the plurality
       of LDPC coded bits of the LDPC codeword are
       provided to a first path of the 3 paths; the last
       n bits of the plurality of LDPC coded bits of the
       LDPC codeword are provided to a second path of the
       3 paths; and the first n bits of the plurality of
       LDPC coded bits of the LDPC codeword are provided
       to a third path of the 3 paths,

(d)   wherein the LDPC coded bits of said LDPC codeword,
       which are output from the three paths, are grouped
       together to form one LDPC coded symbol; such that
       each LDPC coded bit forms part of one of a
       plurality of the LDPC coded symbols,

(e)   wherein the bits from the first path represent the
       most significant bit "MSB" of each symbol, the
       bits from the second path represent the inside
       significant bit "ISB" of each symbol, and the bits

from the third path represent the least
significant bit "LSB" of each symbol,

(f)   two modulation encoders being adapted to operate
      cooperatively such that each modulation encoder
      receives the LDPC coded symbols according to a
      predetermined cycle,

(g)   said predetermined cycle being performed as
      follows:
      the first 4320 symbols and the odd symbols formed
      thereafter are provided to a first modulation
      encoder,
      the even symbols after the first 4320 symbols are
      provided to a second modulation encoder,

(h)   wherein each modulation encoder performs
      modulation encoding on the LDPC coded symbols that
      it receives thereby generating corresponding
      pluralities of LDPC coded modulation symbols;

(i)   each modulation encoder being operable to perform
      a different modulation, said modulations having a
      fixed constellation shape but different
      constellation mappings;

(j)   wherein the first modulation encoder is adapted to
      perform the mapping (0) as specified in
      Figure 19A; and the second modulation encoder is
      adapted to perform the mapping (8) as specified in
      Figure 21A,

(k)   the encoder being adapted to output the coded
      modulation symbols from the modulation encoders as

a signal sequence to form the LDPC coded
modulation signal that is a variable modulation
signal.

2.2   The description as originally filed (page 59, lines 4
       to 8) specifies that the "*variable modulation
       characteristics of the invention may also be applied
       and further explored when considering the LDPC coded
       modulation used in the HNS proposal to the DVB standard.
       That particular LDPC code has 64800 variable nodes with
       4320 degree 13 nodes broken down as follows: 38880
       degree 3 nodes, 21599 degree 2 nodes, and 1 degree 1
       node*".

       Feature (b) of the appellant's claim identifies the
       code only by specifying that it has 64800 variable
       nodes, of which the first 4320 have degree 13 and the
       rest a degree of 3 or less. Thus, the claim relies on a
       more general definition of an LDPC code, as it does not
       specify the degree of all nodes and does not identify
       it as the LDPC code used in the HNS proposal to the DVB
       standard.

       In the Board's opinion, such generalisation is
       admissible in the present case since, as convincingly
       explained by the appellant and shown below, a skilled
       person reading the application realizes that the effect
       achieved by varying the modulation of the LDPC coded
       symbols according to the claim does not depend on the
       use of a particular LDPC code but essentially on the
       fact that the first 4320 variable nodes of the code
       have a degree (13) which is much higher than the
       degrees of the remaining variable nodes.

2.3   As to the other features of the claim, they are fully
        supported by the embodiment shown in Figure 22 and by
        the corresponding passages of the description (page 59,
        line 26 to page 61, line 3).

2.4   In summary, the subject-matter of the claim corresponds
        essentially to the embodiment shown in Figure 22 of the
        application as originally filed and the claim recites
        all the essential features of this embodiment in a
        sufficiently clear and concise manner.

2.5   Hence, the claim of the appellant's request is
        admissible under Article 123(2) EPC and satisfies the
        requirements of Article 84 EPC.

Articles 54 and 56 EPC

3.1   Figures 19A to 21B are diagrams showing 12 different
        Gray maps of an 8 PSK signal constellation which can be
        used to encode groups of three bits of an LDPC codeword.
        As explained on page 58 of the description as
        originally filed (lines 15 to 24), the "*operation of
        such coding may be described when considering a map,
        indicated as Map_i, and the two symbols (a_2, a_1, a_0) and
        (b_2, b_1, b_0). If $a_2 = b_2$ and $a_1 = b_1$, but $a_0 \neq b_0$, and also
        if $Map_i(a_2, a_1, a_0)$ and $Map_i(b_2, b_1, b_0)$ are two consecutive
        numbers, then the map may be characterized as having 1
        weak point at the LSB (Least Significant Bit).
        Similarly, a weak point at the MSB (Most Significant
        Bit) and a weak point at the ISB (Inside Significant
        Bit) may be defined. For example, a weak point at the
        MSB may be defined as follows: if $a_2 \neq b_2$ and $a_1 = b_1$,
        but $a_0 = b_0$, and also if $Map_i(a_2, a_1, a_0)$ and $Map_i(b_2, b_1, b_0)$
        are two consecutive numbers. Also, a weak point at the*

ISB may be defined as follows: $a_2 = b_2$ and $a_1 \neq b_1$, but $a_0 = b_0$, and also if $Map_i(a_2, a_1, a_0)$ and $Map_i(b_2, b_1, b_0)$ are two consecutive numbers."

As pointed out in the description (page 59, lines 8 to 14), the S/P (Serial-to-Parallel) map of the HNS proposal to the DVB standard, which corresponds to Map (4) shown in Figure 20A, has a number of weak points (four) at the LSB which is higher than the number of weak points at the ISB and MSB.

This "*particular map will still provide a relatively high degree of performance to the first 4320 symbols since the LSB of these symbols are degree 13 nodes, which are therefore strongly protected by the corresponding check nodes. However, the remaining 17280 symbols (which include a full 80% of all of the symbols) have both MSB and LSB of only degree 3. Obviously, the LSB bit is much less protected. Therefore, when the information data is a PN (Pseudo-Noise) sequence, which has 1s and 0s evenly distributed in the block, the code behaves sufficiently well. Otherwise, it behaves much worse*" (application as originally filed, page 59, line 14 to 25).

3.2   In order to overcome the above problem, the present application proposes an encoder which, as recited in the claim, comprises two modulation encoders performing mapping according to a predetermined cycle and on the basis of two different maps. In particular, the first 4320 variable nodes with degree 13 are used as the LSB of the three-bit groups to be mapped. The first corresponding 4320 symbols encoded with map (0), which has four weak points at the LSB, two at the ISB and two

at the MSB, are well-protected. However, the remaining
bits of the codeword to be mapped have all the same
degree 3 or lower than 3. In order to "spread" more
evenly the weak points over the bits of the LDPC coded
symbols following the first 4320 symbols, the claimed
encoder changes the mapping on a symbol by symbol basis
using alternatively a map (*i.e.* map (0) of figure 19A)
with four weak points at the LSB and a map (map (8) of
Figure 21A) with four weak points at the MSB.

3.3   The appellant has convincingly argued that using these
two separate mappings according to the cycle recited in
the claim instead of a single mapping significantly
improves the encoder's performance, as shown in the
application. Furthermore, this result did not depend on
the particular code referred to in the description but
only on the fact that the LDPC code had 64800 variable
nodes of which 4320 were of degree 13 and the remaining
of degree 3 and less. The Board sees no reason to doubt
the appellant's assertions.

3.4   It is known in the art that the performance of digital
transmission schemes can be improved by jointly
optimizing coding and modulation (cf. D9,
"Introduction"). It is also known to change mapping
during transmission of LDPC coded bits to take into
account the characteristics of the transmission channel
and/or the transmission requirements of the user (cf.
D8, "Abstract" and section 4.).
However, there is no suggestion in the prior art
available to the Board that it would be advantageous to
use the variable mapping recited in the claim to encode
an LDPC codeword as defined in the claim.

3.5   Hence, the subject-matter of the claim is new according
       to Article 54 and involves an inventive step within the
       meaning of Article 56 EPC.

4.   In the result, the Board finds that the single claim
       according to the appellant's request satisfies the
       requirements of the EPC and that a patent can be
       granted on the basis thereof.

Order

For these reasons it is decided that:

1.   The decision under appeal is set aside.

2.   The case is remitted to the department of first
       instance with the order to grant a patent on the basis
       of the single claim of the new main request filed at
       the oral proceedings of 20 October 2011 and a
       description and drawings still to be adapted.

The Registrar: The Chairman:

C. Moser   M. Ruggiu