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Case Number: T 1513/08 - 3.4.03

Application Number: 99310127.8

Publication Number: 1020921

IPC: H01L 21/336, H01L 29/10, H01L 29/78

Language of the proceedings: EN

Title of invention:
Analog MOSFET devices

Applicant:
LUCENT TECHNOLOGIES INC.

Opponent:
-

Headword:
-

Relevant legal provisions:
EPC Art. 123(2)

Relevant legal provisions (EPC 1973):
EPC Art. 56, 111(1)

Keyword:
"Added subject-matter (yes) - main request"
"Inventive step (yes) first auxiliary request"
"Remittal to the examining division"

Decisions cited:
-

Catchword:
-

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Case Number: T 1513/08 **-** 3.4.03

D E C I S I O N
of the Technical Board of Appeal 3.4.03
of 22 May 2012

Appellant: (Applicant)
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Decision under appeal:
Decision of the Examining Division of the European Patent Office posted 13 March 2008 refusing European patent application No. 99310127.8 pursuant to Article 97(2) EPC.

Composition of the Board:

Chairman: G. Eliasson
Members: T. Häusser
P. Mühlens

Summary of Facts and Submissions

I. The appeal concerns the decision of the examining division to refuse European patent application No. 99 310 127 for lack of inventive step in view of the following document:

D1: US 5,532,508.

II. Oral proceedings were held before the board in the absence of the duly summoned appellant.

III. The appellant had requested in writing that the decision under appeal be set aside and that a patent be granted on the basis of the main request or on the basis of one of the first, second, third or fourth auxiliary requests, all filed with letter dated 20 April 2012.

IV. The wording of claim 1 of the main request and claim 1 of the first auxiliary request reads as follows (labelling $(1)_0$ and $(1)_1$-$(9)_1$ by the board):

Main request:

"An improved silicon MOS transistor integrated circuit comprising a plurality of digital MOS transistor devices and a plurality of analog MOS transistor devices, each of said MOS transistor devices having an MOS gate with a gate threshold voltage and an MOS channel beneath the MOS gate,

$(1)_0$ said digital MOS transistor devices having a channel length comparable to or less than twice the minimum design rule, and

said analog MOS transistor devices having a channel length greater than twice the minimum design rule, each of said analog MOS transistors having:

(a) a silicon substrate, said silicon substrate having a first conductivity type,

(b) a gate dielectric on a said silicon substrate,

(c) a polysilicon gate on said gate dielectric,

(d) a lightly doped drain (LDD) region in said silicon substrate, said LDD region extending in a horizontal direction beneath said polysilicon gate by distance x,

(e) a depletion control implant region of said first conductivity type in said silicon substrate, said depletion control implant region extending beneath said polysilicon gate by distance y, where y > x, that changes the gate threshold voltage by less than 50mV,

(f) sidewall spacers on said silicon gate,

(g) source and drain regions in said silicon substrate,

(h) electrical contacts to said gate source and drain, and

(i) means for applying an analog signal to said silicon gate."

First auxiliary request:

"$(1)_1$ An improved mixed signal silicon MOS transistor integrated circuit comprising

$(2)_1$ a plurality of digital MOS transistor devices and

$(3)_1$ a plurality of analog MOS transistor devices,

$(4)_1$ each of said MOS transistor devices having an MOS gate with a gate threshold voltage and an MOS channel beneath the MOS gate,

(5)$_1$ said digital MOS transistor devices having a gate length comparable to or less than twice the minimum design rule, and

(6)$_1$ said analog MOS transistor devices having a channel length greater than twice the minimum design rule,

(7)$_1$ each of said MOS transistors having a double implanted lightly doped drain structure

(8)$_1$ comprising:

(a) a silicon substrate, said silicon substrate having a first conductivity type,

(b) a gate dielectric on a said silicon substrate,

(c) a polysilicon gate on said gate dielectric,

(d) a lightly doped drain (LDD) region in said silicon substrate, said LDD region extending in a horizontal direction beneath said polysilicon gate by distance x,

(e) a depletion control implant region of said first conductivity type in said silicon substrate, said depletion control implant region extending beneath said polysilicon gate by distance y, where y > x, and,

(f) sidewall spacers on said silicon gate,

(g) source and drain regions in said silicon substrate,

(h) electrical contacts to said gate source and drain, and

(i) means for applying an analog signal to said silicon gate

(9)$_1$ wherein the double implanted lightly doped drain structure increases the gate threshold voltage of the digital MOS transistors by at least 100 mV, and changes the gate threshold voltage of the analog MOS transistors by less than 50 mV."

V. In writing the appellant had argued essentially as follows:

(a) Main request – amendments

Feature $(1)_0$ was consistent with the description, at least page 9, lines 14-17, and did therefore not extend beyond the content of the application as filed. Article 123(2) EPC was thus not violated.

(b) First auxiliary request – inventive step

The closest prior art was the prior art acknowledged in the section "background of the invention" in the application as originally filed. Document D1 could not render the invention obvious since it did not disclose an integrated circuit comprising a plurality of digital MOS transistors and a plurality of analog MOS transistors. In particular, D1 did not disclose the features of claim 1 of the first auxiliary request associated with the effect of the depletion control region on the digital and the analog transistors, respectively.

The common prejudices in the art would prevent a skilled person using the double implanted LDD structure in analog transistors.

The claimed invention involved therefore an inventive step.

Reasons for the Decision

1. Admissibility

The appeal is admissible.

2. Main request - amendments

2.1 The appellant referred to the sentence on page 9, lines 14-17, in the application documents as filed as a basis for feature $(1)_0$ of claim 1 of the main request. That sentence and the preceding two sentences read as follows:

"In mixed signal ICs the transistors that perform digital functions may be designed with a double LDD implant. The purpose of this implant is to avoid adverse short channel effects and maintain the threshold voltage at or above the design value. Therefore the effect of the double implanted LDD in digital technology is to increase the V_T of short channel devices (gate lengths comparable to, or less than twice, the design rule) by a significant value, typically at least 100mV."

The acronym "LDD" is defined on page 2, lines 1-3, to mean 'lightly doped drain'. From the passage cited above it can be inferred that the effect of the double LDD implant in short channel digital transistors is to increase the threshold voltage V_T. Furthermore, transistors are regarded to have a "short channel" if their ***gate length*** is comparable to, or less than twice, the design rule.

According to feature $(1)_0$ of claim 1 of the main request the claimed digital MOS transistor devices are however defined to have a ***channel length*** comparable to or less than twice the minimum design rule. Since the doped source and drain regions are generally extending beneath the gate (cf. Figure 3 of the application), gate and channel lengths are different.

Furthermore, it is sensible to compare the gate length - a visible feature - rather than the channel length to the design rule. Therefore, the use of the expression "gate lengths" in the above passage cannot be regarded as an obvious error, which should in fact read "channel lengths".

Feature $(1)_0$ is therefore not directly and unambiguously derivable from the content of the application as filed.

2.2 Accordingly, the subject-matter of claim 1 of the main request extends beyond the content of the application as filed, contrary to the requirements of Article 123(2) EPC.

3. First auxiliary request – inventive step

3.1 Claim 1 of the first auxiliary request

Claim 1 of the first auxiliary request comprises features which relate by reference to both analog and digital MOS transistor devices, namely features $(4)_1$, $(7)_1$, $(8)_1$, and $(9)_1$. In the following subscripts "a" and "d" are used when these features relate to the analog and digital devices, respectively.

3.2 Closest state of the art

3.2.1 In selecting the closest state of the art, the first consideration is that it should be directed to the same purpose or effect as the invention. Otherwise it cannot lead the skilled person in an obvious way to the claimed invention (see "Case Law of the Boards of Appeal of the European Patent Office", 6th edition 2010, I.D.3.2).

The claimed invention relates to a mixed signal (i.e. analog and digital) silicon MOS transistor integrated circuit so that the purpose of the invention can be regarded to perform the functions of the integrated circuit.

3.2.2 In the decision under appeal document D1 was regarded as the closest state of the art. D1 relates to a single circuit element, a MOS type field effect transistor with a double implanted LDD structure. Although document D1 does not disclose any applications for the MOS transistor, the skilled person – a semiconductor physicist – would infer from the size and design of the transistor that it would be suitable in a digital integrated circuit. However, the use of the MOS transistor in a mixed signal integrated circuit is not disclosed in D1.

3.2.3 The appellant considers the prior art originally acknowledged in the section "background of the invention" of the description as the closest state of the art. That part of the description deals primarily with the efforts, concerns, and problems encountered in

the integrated circuit technology, - a mixed analog and digital integrated circuit is not mentioned.

3.2.4 In his letter dated 8 November 2007 submitted during the examination proceedings, the appellant had agreed with the examiner that it would be obvious, in a mixed signal circuit to design some MOS devices, those that perform digital functions, with channel length L, and other MOS devices, those that perform analog functions, with channel length 2L. Thus the appellant did not contest that a mixed signal MOS transistor integrated circuit belonged to the state of the art.

Furthermore, the board regards such a mixed signal integrated circuit to be notoriously known at the priority date of the application. As such a circuit is directed to the same purpose as the invention it is regarded to constitute the closest state of the art.

3.3 Objective technical problem

The subject-matter of claim 1 of the first auxiliary request differs from a conventional mixed signal MOS transistor integrated circuit at least in comprising the features $(6)_1$, $(7)_1$, $(8)_{1,a}$, and $(9)_1$.

Starting from D1 as closest state of the art the examining division held in the appealed decision that the claimed invention solved different partial problems. The board regards such a division of the technical problem to be inappropriate in the present case for the following reasons: Features $(6)_1$, $(7)_{1,a}$, $(8)_{1,a}$, and $(9)_{1,a}$ all relate to the analog transistor devices. Furthermore, features $(7)_{1,d}$ and $(9)_{1,d}$

contribute to setting the scale of the "minimum design rule", which is also used for defining the channel length of the analog transistor devices (feature $(6)_1$). The differing features mentioned above are therefore functionally interdependent.

The effect of the above features is to increase the output impedance and thus the gain in the analog MOS transistor devices without significantly affecting the threshold voltage, and to avoid short channel effects in the digital MOS transistor devices thus ensuring their proper functioning. The objective technical problem is therefore to perform analog amplification with good performance while minimizing the device size (see pages 1 and 2 of the description of the application).

3.4 Obviousness

3.4.1 In the decision under appeal the examining division regarded the first ion implanted layer 5 of D1 as the claimed depletion control implant region. Furthermore, Figure 11 of D1 showed that for a channel length of 0.5µm the difference between the threshold voltage of a MOS transistor without depletion control implant and one with a depletion control implant of $1x10^{13}/cm^2$ had a value of about 40mV. Therefore - according to the opinion of the examining division - the skilled person would solve the problem of improving the characteristics of the MOS transistor by attempting to minimize the negative impact of the depletion control implant region on the threshold voltage of the transistor thus arriving at the feature that the

depletion control implant changed the gate threshold voltage V_t by less than 50mV.

3.4.2 Document D1 is concerned (see column 1, third paragraph; column 3, line 19 – column 5, line 52) with the drawback of conventional field effect transistors with LDD structure and submicron channel length that a threshold voltage and a source/drain breakdown voltage are lowered owing to a short channel effect. D1 proposes a MOS type field effect transistor with a modified LDD structure. A gate oxide film 3 is formed on a P or N type semiconductor substrate 1 and a polysilicon gate electrode 4 is formed on the oxide film 3. Impurity ions having the same conductivity as the semiconductor substrate are implanted in the substrate 1 to form a first implanted layer 5 for controlling the source/drain breakdown voltage. Furthermore, impurity ions having the same conductivity as the semiconductor substrate are implanted in the substrate to form a second implanted layer 6 for controlling the threshold voltage. Finally, impurity ions having the same, respectively opposite conductivity to the substrate are implanted to form third and fourth implanted layers 7 and 9, which form an impurity diffusion layer working as the source and drain region.

3.4.3 As described above, document D1 is concerned with increasing the threshold voltage and source/drain breakdown voltage in transistors having submicron channel length, but not with improving the amplification characteristics of analog transistors. The board agrees that it would be sensible to apply the teaching of D1 to the digital transistors having short

channel lengths. However, the skilled person would not consider document D1 when attempting to solve the posed technical problem of improving analog amplification.

3.4.4 However, assuming for the sake of argument that the skilled person were to consider the teaching of document D1 also for the analog transistors, the board is of the opinion that he would not be led to the claimed subject-matter. In particular, short channel effects would not be regarded as a problem for the larger analog MOS transistor devices. This would only be an issue for the smaller digital MOS transistors. Hence, if the skilled person might have considered designing the analog MOS transistor devices with longer channels than the digital MOS transistor devices, he would see no reason for applying an ion implanted layer for controlling the source/drain breakdown voltage or the threshold voltage.

Accordingly, the subject-matter of claim 1 of the first auxiliary request involves an inventive step over document D1.

3.4.5 None of the other documents of the state of the art on file contains a teaching that would lead the skilled person in an obvious way to the subject-matter of claim 1 of the first auxiliary request.

Claims 2 to 5 are dependent on claim 1 providing further limitations of the integrated circuit according to claim 1. Accordingly, the board is satisfied that the subject-matter of claims 1 to 5 of the first auxiliary request involves an inventive step under Article 56 EPC 1973.

4. Remittal to the department of first instance

4.1 It remains to be considered whether the first auxiliary request complies with the other requirements of the EPC, for example whether feature $(8)_{1,d}$ (i.e. that the digital MOS transistor devices have the structure (a)-(i)) complies with the requirements of Article 123(2) EPC. Since the appellant was not represented at the oral proceedings before the board, these other requirements of the EPC could not be discussed with him.

4.2 In view of the above, the board finds it appropriate to remit the case to the department of first instance for further prosecution under Article 111(1) EPC 1973.

Order

For these reasons it is decided that:

1. The decision under appeal is set aside.

2. The case is remitted to the department of first instance for further prosecution.

The Registrar: The Chairman:

S. Sánchez Chiquero G. Eliasson