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Datasheet for the decision
of 24 February 2012

Case Number: T 1272/08 - 3.5.06

Application Number: 03775521.2

Publication Number: 1561160

IPC: G06F 9/318

Language of the proceedings: EN

Title of invention:
A configurable processor architecture

Applicant:
Imagination Technologies Limited

Headword:
Configurable processor architecture/IMAGINATION

Relevant legal provisions:
EPC Art. 123 (2)

Relevant legal provisions (EPC 1973):
EPC Art. 56, 84

Keyword:
"Clarity - no"
"Added subject matter - yes"
"Inventive step - no"

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Beschwerdekammern   Boards of Appeal   Chambres de recours

Case Number: T 1272/08 - 3.5.06

D E C I S I O N
of the Technical Board of Appeal 3.5.06
of 24 February 2012

Appellant:
(Applicant)

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Representative:

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Decision under appeal:

**Decision of the Examining Division of the
European Patent Office posted 7 February 2008
refusing European patent application
No. 03775521.2 pursuant to Article 97(2) EPC.**

Composition of the Board:

Chairman: D. H. Rees
Members: M. Müller
                   W. Sekretaruk

Summary of Facts and Submissions

I.   The appeal lies against the decision of the examining
        division, dispatched on 7 February 2008, to refuse
        European patent application no. 03775521.2 for lack of
        an inventive step, Article 56 EPC 1973, in view of
        inter alia the following documents:

        D1:   Arndt M. *et al.*, "Software radio: the challenges
               for reconfigurable terminals", Ann. Télécommun.,
               57, nr. 7-8, p. 570-612, July 2002
        D5:   Software Defined Radio Forum, "Requirements for
               Radio Software Download for RF Reconfiguration",
               SDRF-02-A-0007-V0.00, 13 November 2002
        D6:   Hansson A. *et al.*, "Global Positioning System in a
               Digital Signal Processor for the TMS320 Platform",
               Application Report, Luleå University of Technology,
               Luleå, Sweden, April 2001

II.   The decision referred to the following documents:

        description, pages   1-12 as published
        drawings, sheets   1, 2 as published
        claims, no.   1-17 according to the main or
                             secondary requests, both filed with
                             telefax of 28 December 2007

III.   A notice of appeal against this decision was received
        on 17 April 2008, the appeal fee being paid on the same
        day. A statement of grounds of appeal was received on
        17 June 2008.

IV.   According to the notice of appeal, the decision to re-
        fuse the European Patent Application is "appealed in

its entirety". In the grounds of appeal, the appellant
argues why the decision was wrong to reject the main
request. Neither the notice of appeal nor the statement
of grounds of appeal specifies the appellant's requests
explicitly, and neither mentions the secondary request
at all.

V.   With summons to oral proceedings, the board informed
       the appellant of its preliminary opinion according to
       which the main request lacked clarity, Article 84 EPC
       1973, went beyond the application as originally filed,
       Article 123 (2) EPC, and lacked an inventive step,
       Article 56 1973. The board further expressed its doubts
       as to whether the secondary request as refused was
       maintained in the appeal, but also its preliminary
       opinion that the secondary request would lack an inven-
       tive step, too.

VI.   Neither amendments nor arguments were filed in response
       to the summons. Instead, the appellant informed the
       board - with telefax of 9 December 2011 and, for con-
       firmation, with letter dated 15 February 2012 - of its
       intention not to be represented at the oral proceedings.

VII.   Claim 1 according to the main request reads as follows:

       "A multi-standard broadcast or receiver processor com-
       prising a programmable modulation and coding processor
       (1) closely coupled to a data memory (2), a memory (4)
       for storing instruction words for the programmable pro-
       cessor, a direct memory access unit (3) (DMA) coupled
       to the data memory (2), at least one input side
       dedicated processor (30) coupled between a data input
       and the memory access unit and at least one output side

dedicated processor (31) coupled between the memory access unit and a data output, wherein the input and output side processors perform operations common to many signal standards on input and output data and the programmable processor performs operations specific to individual standards, and wherein the programmable processor is loaded with different sets of instruction words in dependence on the standard of a received signal, and wherein the inputs and outputs to the programmable processor are made by the DMA unit via the closely coupled memory unit."

VIII.   Oral proceedings thus took place in the absence of the appellant. At the end of the oral proceedings, the chairman announced the decision of the board.

Reasons for the Decision

1.   The duly summoned appellant did not attend the oral proceedings. In accordance with Article 15 (3) RPBA the board relied for its decision only on the appellant's written submissions. The board was in a position to decide at the conclusion of the oral proceedings, since the case was ready for decision (Article 15 (5,6) RPBA), and the voluntary absence of the appellant was not a reason for delaying the decision (Article 15 (3) RPBA).

2.   The reasons for this decision are based on the preliminary opinion communicated to the appellant with the summons to oral proceedings.

Admissibility and extent of the appeal

3.   As regards the main request, the appeal is clearly in
        conformance with Articles 106-108 and Rule 99 EPC and
        therefore admissible (see also points I and II above).

4.   In the summons to oral proceedings, the board had ob-
        served that the grounds of appeal was limited to the
        main request and did not contain any arguments in
        favour of the secondary request, and expressed its
        doubts as to whether the appellant intended to maintain
        the secondary request in appeal at all. The appellant
        has not submitted anything in response to remove the
        board's doubt. The board therefore considers that the
        appellant's request is to set aside the decision and to
        grant a patent based on the main request only.

The Invention

5.   The application relates to a processor architecture
        which is suitable for a broadcast receiver (*e.g.* for
        television) or communication system (*e.g.* a mobile
        phone).

5.1   The invention according to claim 1 of the main request
        specifies a "multi-standard broadcast or receiver pro-
        cessor" comprising a central "programmable modulation
        and coding processor" (MCP), at least one "input side
        dedicated processor" and at least one "output side
        dedicated processor", and a direct memory access (DMA)
        unit. It is specified that the MCP is closely coupled
        to data memory, that the DMA unit is coupled between
        that data memory and the input and output side pro-
        cessors, and that the DMA unit makes input and outputs
        to the processor via that data memory.

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5.2   The input side and output side processors are specified
        to perform operations "common to many signal standards"
        while the MCP is to perform operations "specific to
        individual standards" according to program instructions
        which are loaded "in dependence of a received signal".

Articles 84 EPC 1973 and 123 (2) EPC

6.   Claim 1 as originally filed referred to a processor
        system comprising, *inter alia*, a programmable VLIW pro-
        cessor and a "memory access unit". The terms "pro-
        grammable VLIW processor" and "memory access unit" were
        later replaced by "programmable modulation and coding
        processor" (MCP) and "direct memory access unit".

6.1   The board notes that further occurrences of the term
        "programmable processor" and "memory access unit" in
        the claims (esp. in claim 1, page 13, lines 13-14, 17,
        19 and 22) were not correspondingly amended. This de-
        ficiency as regards the processor renders unclear which
        is the difference, if any, between the MCP and the pro-
        grammable processor, Article 84 EPC 1973.

6.2   The application distinguishes between the MCP (fig. 1,
        no. 10) and one of its components, the programmable
        processor (fig. 1, no. 1). The distinction between
        these processors is blurred by claim 1. This causes
        clarity problems such as whether the MCP can be called
        "closely coupled" to its components, Article 84 EPC
        1973.

6.3   Due to this clarity problem, claim 1 allows the inter-
        pretation that the "programmable processor" refers to
        the MCP. According to this interpretation, however, the

claimed feature that "the inputs and outputs to the
programmable processor are made by the DMA unit" is not
supported by the application as originally filed. The
DMA unit being a component of the MCP, it is clear from
the application (fig. 1) that inputs to the MCP (10)
are not made via the DMA unit, but only inputs and out-
puts to the programmable processor (1) within the MCP
(10) are. The board therefore concludes that claim 1 of
the main request offends against Article 123 (2) EPC.

Inventive Step

7.   Notwithstanding the above-mentioned deficiencies of the
        wording of claim 1 under Articles 84 EPC 1973 and 123
        (2) EPC, the board deems it appropriate to assess in-
        ventive step of the claimed invention as interpreted in
        view of the description and drawings. According to this
        interpretation the "programmable modulation and coding
        processor (1)" is taken to refer not to the MCP but to
        the component of the MCP referred to as "programmable
        processor" in figure 1 and elsewhere in claim 1.

8.   It is common ground that D1 constitutes the closest
        piece of prior art at hand.

8.1   D1 addresses the problem of facilitating the access to
        multiple telecommunication standards using the same mo-
        bile device (see abstract and introduction) and disclo-
        ses a multi-standard receiver processor system. This
        system comprises a central digital signal processor DSP
        which performs, *inter alia*, modulation and coding (cf.
        figs. 6 and 11, Modem; and p. 589, penult par.) and
        which is coupled to input side and output side pro-
        cessors (cf. the RF and Message Processing components

depicted in fig. 6 and 11, pp. 583 and 590, and con-
tained in table II, p. 588; see also figs. 10 and 12 on
pp. 588 and 591). The input and output side processors
perform operations common to many signal standards (cf.
e.g. p. 587, last par.) whereas the central DSP per-
forms operations specific to individual standards (see
esp. p. 589, penult. par.). The DSP comprises closely
coupled memory including data and program instructions
(cf. p. 583, penult. par., lines 4-5).

8.2   D1 discloses that the DSP may have to be reconfigured
        for a different standard and mentions the change of
        standard while roaming (cf. *e.g.* p. 572, 4th par.,
        "inter radio access roaming"), but does not detail how
        the need for reconfiguration is to be detected (cf. par.
        bridging pp. 589-590). D1 thus does not disclose that
        the loading of instruction words is "in dependence on
        the standard of a received signal".

8.3   D1 further does not mention a direct memory access unit
        or its use to control data transfer between the input
        and output side processors and the DSP.

9.   The decision under appeal argues that these two diffe-
        rences address essentially unrelated problems of pro-
        cessor reconfiguration on the one hand and efficient
        inter-processor communication on the other so that
        their inventive merit can be assessed separately. The
        board agrees with this argument and the grounds of
        appeal do not challenge it either.

10.   The impugned decision (cf. point 4.3, item b, and point
        4.6) finds the first difference (point 8.2) to lack an
        inventive step over D1, *inter alia* in view of D5. The

statement of grounds of appeal does not address this
difference or its inventive merit, nor does it mention
the pertinent part of the reasoning in the decision un-
der appeal at all. In the summons to oral proceedings
the board expressed its perception that the appellant
did not intend to challenge the decision in this res-
pect, and the appellant did not contradict this percep-
tion. Therefore, the board concludes that it is not
part of the appellant's case, Article 12 (2) RPBA, to
establish inventive step of the claimed invention by
virtue of this first difference. Only for completeness
the board points out that, as argued in the summons to
oral proceedings, it agrees with the impugned decision
that this difference indeed does not establish an in-
ventive step of the claimed invention over D1.

11.   The second difference (point 8.3) improves the data
        processing efficiency of the multi-processor system
        according to D1. The board agrees with the decision
        that DMA units are commonly used for just this effect
        in multi-processor systems (cf. decision, p. 5, lines
        9-11). Whether a DMA unit is also implicitly disclosed
        in D1 may be left open.

11.1   The decision under appeal finds the second difference
        to lack an inventive step over D1, *inter alia* in view
        of D6.

11.2   The grounds of appeal (last par., line 10) state that
        "the documents come from different fields". Furthermore,
        they argue (last par., lines 5-11) that the invention,
        by "not requir[ing] a separate memory to act as a swing
        buffer ... makes more efficient use of the silicon"
        than a combination of D1 and D6 would suggest.

11.3   D6 discloses a Global Positioning System GPS in a Digi-
        tal Signal Processor for the TMS320 DSP Platform (see
        title) based on the "software radio concept" (sec. 1.2)
        and D6 also anticipates its integration into a "multi-
        mode radio" as used in the "wireless area" (p. 4, 2nd
        par., lines 2-6; cf. also sec. A.3). The board reads
        this an explicit indication to integrate the GPS of D6
        into a multi-standard mobile communication device such
        as that of D1. Also D1 itself discloses the idea of in-
        tegrating GPS in such a device (see p. 571, last line).
        Therefore, the board does not consider D1 and D6 to be
        from different fields.

11.4   In the board's view, the skilled person setting out to
        solve data processing efficiency in the multi-standard
        device of D1 would extend its search to devices with a
        similar architecture expecting to find solutions which
        are applicable to the system of D1 and therefore would
        indeed consider D6.

11.5   D6 addresses the problem of transferring data samples
        from the input processors (FPGA) to the DSP in an effi-
        cient manner and proposes as a solution to use the DMA
        controller on the DSP (cf. p. 9, 1st and 2nd pars.). D6
        also discloses that the DMA controller implements dual
        buffering (also known as ping-pong or swing buffering)
        in the internal - *i.e.* closely coupled - memory of the
        DSP (p. 11, 3rd par.). D6 thus also does not need any
        "separate memory to act as a swing buffer" and thus
        makes as efficient use of the silicon as the invention
        in this respect (cf. grounds of appeal, last par.,
        lines 5-7). The board further takes D6 to disclose that
        "inputs and outputs to the ... processor are made via

the closely coupled memory" which was disputed by the appellant in the communication dated 28 December 2007.

11.6   In the board's view it is obvious for the skilled person that the data efficiency achieved by this solution does not depend on the nature of the data and would thus carry over immediately to the system of D1. In the board's judgement it is also well within the competence of the skilled person to adopt the same technique for the output processors. The board hence considers the difference according to point 8.3 to be insufficient to establish an inventive step of the claimed invention over D1 in view of D6.

11.7   In summary, claim 1 of the main request lacks an inventive step, Article 56 EPC 1973, over D1 in view of the prior art, especially D5 and D6.

Order

For these reasons it is decided that:

The appeal is dismissed.

The Registrar: The Chairman:

B. Atienza Vivancos   D. H. Rees

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