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Datasheet for the decision of 6 April 2011

Case Number: T 1197/08 - 3.4.02

Application Number: 01118909.9

Publication Number: 1180716

IPC: G02F1/1362, G02F1/1368, G02F1/1345, G02F1/1335

Language of the proceeding: EN

Title of invention:
Thin film semiconductor device and liquid crystal display unit, and fabrication methods thereof

Applicant:
Sony Corporation

Headword:

Relevant legal provisions:
EPC Art. 56

Keyword:
Inventive step (yes)

Decisions cited:

Catchword:

Europäisches Patentamt | European Patent Office | Office européen des brevets

Beschwerdekammern | Boards of Appeal | Chambres de recours

Case Number: T 1197/08 - 3.4.02

D E C I S I O N
of the Technical Board of Appeal 3.4.02
of 6 April 2011

Appellant: Sony Corporation
(Applicant)
Representative: Müller - Hoffmann & Partner
Patentanwälte
Innere Wiener Strasse 17
81667 München (DE)

Decision under appeal: Decision of the Examining Division of the European Patent Office posted 31 January 2008 refusing European application No. 01118909.9 pursuant to Article 97(2) EPC.

Composition of the Board:

Chairman: A. Klein
Members: M. Stock
D. Rogers

Summary of Facts and Submissions

I. The appellant has appealed against the decision of the examining division refusing European patent application number 01 118 909.9 on the ground that its subject-matter lacked an inventive step within the meaning of Article 56 EPC in view of the following documents:

D1: Patent Abstracts of Japan, vol. 1997, no. 01, 31 & JP 08 234239 A

D4: EP-A-0 997 769

II. The appellant has requested to set the decision of the examining division aside and to grant a patent on the basis of claims according to a main request filed with letter dated 26 October 2007, first to third auxiliary requests amended during the appeal proceedings appeal.

Appellant's arguments can be summarised as follows:

An electrical connection between the gates, i.e. the gate interconnection, was mandatory in the present type of device. Hence, there was no unnecessary connection in Fig. 8 of D1 in contradiction to the statement of the Examining Division when formulating the objective technical problem. An objective definition of the problem to be solved by the invention should normally start from the problem described in the application documents. In the present case Fig. 6 of the application documents (known device) and the embodiment of Figs. 5 and 8 of D1 had the same problem in common. In Fig. 6 of the application documents a gap (GAP) had to be provided between the gate interconnection and an upper electrode of the auxiliary capacitor, both

elements being formed within the same semiconductor thin film 14. Such a gap was also required in the device shown in Figs. 5 and 8 of D1. Here, the gate wiring pattern 10 (corresponding to the gate interconnection and the gate itself) and the auxiliary capacitance pattern 11 (corresponding to the upper electrode of the auxiliary capacitance) were made on the same layer. Hence, a gap was mandatory between the upper electrode of the auxiliary capacitance and the gate interconnection (gate wiring pattern 10) to avoid short-circuits. As could be gathered from Fig. 7 of the application and the related description part on page 9, such a parallel layout of gate interconnection and upper auxiliary capacitance electrode made it difficult to improve the pixel opening rate whilst also ensuring the area of the auxiliary capacitance. Thus, the objective technical problem might be formulated as providing a gate interconnection allowing for an improved pixel opening rate.

For solving this problem the skilled person had no incentive to consider document D4 when starting from D1 because D4 did not provide any benefits vis-à-vis the device of Fig. 8 of D1 that would help to solve the objective technical problem. The arrangement of the gate interconnection in D4, i.e. a polysilicon layer for gate line 141 in Fig. 4 corresponded to gate wiring layer 10 of Fig. 8 of D1 (reference was made also to cross-sectional view shown in Fig. 5 and to the fact that the gate wiring layer 10 connected neighbouring gates by a gate line which ran behind or before the drawing plane of Fig. 5).

Hence, both documents, D1 and D4, had the same gate interconnection as illustrated in the known device of Fig. 6 of the application documents, this gate

interconnection being the starting point for the formulation of the objective technical problem. As document D4 does not differ from document D1 with regard to the gate interconnection, document D4 would not have been considered by the skilled person as it does not give any hint to solve the objective technical problem of improving the pixel opening rate.

Thus, the subject-matter of claim 1 was based on an inventive step.

III. In preparation for the oral proceedings requested by the appellant, the Board made preliminary non-binding comments.

The prior art described in the present application in connection with Figures 5 and 6 corresponded to document D4. While Figure 3 in D4 was almost identical to Figure 5 in the present application, a figure corresponding to Figure 6 in the present application was not found in D4. In any case D4, see Figures 3 and 4 with the associated description, disclosed a thin film semiconductor device comprising all features indicated in claim 1 according to the main request and thus being prejudicial to the novelty of the claimed subject-matter.

IV. In a response to the communication of the Board the appellant stated its disagreement with the Board's preliminary comment according to which D4 provides disclosure for the feature (reference numerals used in D4 are indicated in parenthesis)

said first electrodes (14) are further connected to said second conductive light shield layer (4).

Neither Fig. 3 nor Fig. 4 illustrated the above feature. According to the plan view of Fig. 4 of D4, the first electrodes arranged along a line parallel to the gate line 141 as well as their interconnection were formed of one continuous second polysilicon layer 142 for the auxiliary capacitance. In view of the continuous arrangement of the second polysilicon layer in the shape of a conductive line with protruding portions, the skilled practitioner would not conclude that a potential of the first electrodes will be fixed from outside of the pixel array via this conductive polysilicon line. The plan view of Fig. 4 also lacked any contacts on the first electrodes to provide a connection with the light shield layer such as contact CCN illustrated in Fig. 6 of the present application.

Moreover, paragraph [0031] of D4 provided further details with regard to the mask layer and taught

specifically that the light-shielding mask layer 4M shall have a fixed potential, which is, for example, equal to the potential of the counter electrode 6, while the light-shielding pad layer 4P shall be so interposed between the pixel electrode 8 and the lead electrode 12B as to enhance the electric connection between the two (see Fig. 3).

Thus, also paragraph [0031] lacked any disclosure for or hint to the above feature.

Therefore, the appellant was of the opinion that the subject-matter of claim 1 of the main request was novel vis-à-vis D4.

V. Claim 1 according to the main request reads as follows:

1. A thin film semiconductor device comprising:
a plurality of signal interconnections (12) and a plurality of gate interconnections crossing said signal interconnections;
pixels disposed at crossing points between said signal and gate interconnections, each of said pixels including at least a pixel electrode, a thin film transistor for driving said pixel electrode and an auxiliary capacitor (13) for holding signal charges written from said signal interconnection into said pixel electrode via said thin film transistor, each of said thin film transistors comprising a source, a drain and a gate electrode (G) and each of said auxiliary capacitors comprising a first (14) and a second electrode (10), said second electrode (10) being connected to said drain;
a first conductive light shield layer (5) formed on an insulating substrate (1) and configured and adapted for shielding said thin film transistors from external light from below;
wherein
said sources are connected to a respective signal interconnection;
said drains are connected to a respective pixel electrode;
said gate electrodes are formed in a third conductive layer (14) different from said first conductive light shield layer;
said first electrodes are formed in said third conductive layer;
characterized by
a second conductive light shield layer configured and adapted for shielding said thin film transistors from light from above, wherein

said second electrodes are mutually distinctly formed in a semiconductor layer formed intermediate said first conductive light shield layer and said third conductive layer,
said first electrodes are further connected to said second conductive light shield layer; and
said gate interconnections are formed in said first conductive light shield layer;
said gate electrodes are mutually distinctly formed in said third conductive layer; and
said first electrodes are mutually distinctly formed in said third conductive layer.

Reasons for the Decision

1. Amendments

The claims according to the present main request already formed the basis of the decision of the examining division. In view of the fact that the examining division only rejected an auxiliary request filed during the oral proceedings under Article 123(2) EPC it can be assumed that the claims according to the main request were considered admissible under Article 123(2) EPC. In fact the claim wording reflects in detail the layered structure of a thin film semiconductor device having a pixel structure provided by the crossing points of signal and gate interconnections as shown in the figures. Therefore the Board is satisfied that the requirements of Article 123(2) EPC are met with respect to the main request.

2. Novelty and inventive step

The Board can accept the appellant's arguments that the feature

said first electrodes are further connected to said second conductive light shield layer

would not be derived from D4 by a person skilled in the art. This is due to the fact that in the device of D4 (see Figure 3 corresponding to Figure 5 of the present application) a gap (GAP) must be provided between the gate interconnection and an upper electrode of the auxiliary capacitor both formed within the same semiconductor layer 14, as is illustrated in Figure 6 which is a plan view of Figure 5 (Figure 3 of D4). Such a gap avoids short-circuits between the gate interconnection and the upper electrode of the auxiliary capacitor. Evidently, such a gap is also needed between the gate wiring pattern 10 of the transistor Tr and the auxiliary capacitance pattern 11 (Cs) in the device described in D1, see Figure 5.

The invention is based on the recognition that the design of using one layer for the gate interconnection and the upper electrode of the auxiliary capacitance, which requires the provision of a gap limits the pixel opening rate. From Figure 7 with the description on page 9 it can be seen that as the pixel opening rate is increased, the area of the auxiliary capacitance is sacrificed. This problem is solved by a design in accordance with the definition of the present invention in claim 1 according to the main request, in which the gate interconnection and the upper electrode of the auxiliary capacitance are formed as separate layers.

Clearly, documents D1 and D4 both favouring the one-layer solution employing a gap do not hint at the

design of forming gate interconnections and upper electrodes of the auxiliary capacitances in separate layers. Therefore the subject-matter of claim 1 according to the main request was not obvious from a combination of D1 with D4. This view is not changed by the other documents cited in the European search report, which are less relevant.

Therefore the conclusion is reached that the subject-matter of claim 1 according to the main request is novel and involves an inventive step.

3. Further issues

The dependent claims 2 and 3 are related to embodiments of the thin film semiconductor device defined in claim 1, claim 2 being directed to a liquid crystal display unit comprising such a thin film semiconductor device.

The description has been adapted to the claims as amended, and supplemented by a reference to document D4, and as such also meets the requirements of the EPC.

In its response (31.03.2011) to a phone conversation (23.03.2011), in which the Board communicated its intention to allow claim 1 of the main request, the appellant requested to cancel the oral proceedings appointed and to grant a patent on the basis of the main request, i.e. on claims, description and drawings as recited below. Since the main request could be granted there was no need to consider the auxiliary requests. The oral proceedings were cancelled on 01.04.2011, accordingly.

Order

For these reasons it is decided that:

The decision under appeal is set aside.

The case is remitted to the first instance with the order to grant a patent in the following version:

Description:
Pages 1 to 8, 11, 12, 14 to 26 as originally filed.
Pages 9, 9A, 13 and 27 filed with letter dated 29.11.2004.
Pages 9B, 9C and 10 filed with letter dated 26.10.2007.

Claims:
No. 1 filed with letter dated 26.10.2007.
Nos. 2 and 3 filed with letter dated 03.05.2006.

Drawings: 1/7 to 7/7 as originally filed.

The Registrar: The Chairman:

M. Kiehl A. Klein