Internal distribution code:
(A) [ ] Publication in OJ
(B) [ ] To Chairmen and Members
(C) [ ] To Chairmen
(D) [X] No distribution

Datasheet for the decision
of 20 June 2012

Case Number:	T 0649/08 - 3.5.02
Application Number:	04258172.8
Publication Number:	1677421
IPC:	H03L 7/08, H03L 1/02
Language of the proceedings:	EN

Title of invention:
Selectively pretuning and updating a phase lock loop

Applicant:
Alcatel-Lucent Deutschland AG

Opponent:
–

Headword:
–

Relevant legal provisions:
EPC Art. 54, 123(2)

Relevant legal provisions (EPC 1973):
–

Keyword:
"Amendments - added subject-matter (yes)"
"Novelty - main request (no) - auxiliary request (no)"

Decisions cited:
–

Catchword:
–

C8021.D
EPA Form 3030   This datasheet is not part of the Decision.
                  It can be changed at any time and without notice.

Case Number: T 0649/08 - 3.5.02

D E C I S I O N
of the Technical Board of Appeal 3.5.02
of 20 June 2012

Appellant: (Applicant)	Alcatel-Lucent Deutschland AG Lorenzstrasse 10 D-70435 Stuttgart (DE)
Representative:	Michalski Hüttermann & Partner Patentanwälte Neuer Zollhof 2 D-30221 Düsseldorf (DE)
Decision under appeal:	**Decision of the Examining Division of the European Patent Office posted 12 November 2007 refusing European application No. 04258172.8 pursuant to Article 97(1) EPC 1973.**

Composition of the Board:

Chairman:	M. Ruggiu
Members:	M. Léouffre
	P. Mühlens

C8021.D

Summary of Facts and Submissions

I.   The applicant lodged an appeal against the decision of
      the examining division posted 12 November 2007, to
      refuse the European patent application No. 04258172.8.

II.   The examining division held that the application,
      comprising the claims filed on 19 October 2007, did not
      meet the requirements of Articles 54 and 56 EPC having
      regard to the prior art (D1 to D5) cited in the search
      report.

III. In a communication posted 2 February 2012 summoning the
      appellant to oral proceedings, the Board indicated that
      some amendment made to claim 1 might contravene
      Article 123(2) EPC and that claims 1 and 9 might not
      meet the requirements of Article 84 EPC.

      The Board referred additionally to the following state
      of the art:

      D6 = US 4 847 569 A; and
      D7 = GB 2 389 254 A

      and informed the appellant of its preliminary opinion
      that the subject-matter of claims 1, 2 to 4 and 9 would
      lack novelty having regard to D6 and that D7 might be
      considered for the assessment of inventive step since
      it addressed the same problem (cf. page 1, lines 1 to
      14; page 3, lines 8 to 17 and page 4, lines 11 to 14)
      as the present application, namely: providing a phase
      lock loop system (PLL) for mobile communication systems
      (cf. paragraph [0002] of the application) wherein a
      complete desired frequency span is separated into sub-

ranges, and wherein the PLL can adapt to the temperature changes (cf. paragraphs [0004], [0006] and [0007]).

IV.   With a letter dated 8 June 2012 the appellant informed the Board that their participation to the oral proceedings were not intended, and filed "an argumentation concerning the Decision to refuse a European Patent application of 12 November 2007, and an auxiliary request comprising a set of amended claims for replacing all previous claims".

V.   Oral proceedings before the board took place on 20 June 2012, at which the appellant were not represented.

The appellant requested in writing that the decision under appeal be set aside and that a patent be granted on the basis of claims 1 to 10 of the request filed with letter of 19 October 2007 (main request) or on the basis of claims 1 to 10 of the auxiliary request filed with letter of 8 June 2012.

VI.   Claim 1 of the main request reads as follows:

"A phase lock loop (115) for providing an output signal having a frequency selected based on comparison of an input signal frequency and a feedback signal frequency, the feedback signal being produced in response to the output signal comprising:
a digital storage (140) to store information indicative of a first frequency and first voltage/current information associated with the first frequency;
an oscillator (150) to provide an oscillator frequency that is used to generate the output frequency of the

phase lock loop (115); and

a frequency generator circuit (125) capable of producing at least one control signal based on the first frequency and the first voltage/current information, wherein said oscillator is configured to provide said first frequency in response to said at least one control signal, characterized in that: the frequency generator circuit (125) is configured to cause said oscillator to adapt the oscillator frequency based on said first frequency in response to a trigger signal by determining a change in said at least one control signal using said digital storage and selectively updating said information relating to said first frequency in the digital storage (140)."

Claim 9 of the main request reads as follows:
"A method for selectively pretuning and updating a phase lock loop, the method characterized by: storing a plurality of desired frequencies including a first and a second desired frequency to adapt said phase lock loop;
holding at least one actual voltage/current to enable a self-calibration in said phase lock loop when generating said plurality of desired frequencies; and in response to a trigger signal, steering an oscillator associated with said phase lock loop to said first desired frequency of said plurality of desired frequencies and determining a change in at least one control signal based on said stored information relating to said first desired frequency and selectively updating said information relating to said first desired frequency."

Claims 2 to 8 are dependent on claim 1. Claim 10 concerns an apparatus comprising means for performing the steps of claim 9.

VII.   Claim 1 of the auxiliary request reads as follows:

"A phase lock loop (115) comprising:
a digital storage (140) to store information indicative of a first frequency and first voltage/current information associated with the first frequency;
an oscillator (150) to provide an oscillator frequency; and
a frequency generator circuit (125) capable of producing at least one control signal based on the first frequency and the first voltage/current information, wherein said oscillator is configured to provide said first frequency in response to said at least one control signal, characterized in that:
the frequency generator circuit (125) is further configured to provide a trigger signal to indicate that information indicative of a second frequency and second voltage/current information associated with the second frequency are to be stored in the digital storage (140), wherein the trigger signal is provided to cause an update of the digital storage (140) from the first frequency to the second frequency."

Claim 9 of the auxiliary request reads as follows:
"A method for selectively pretuning and updating a phase lock loop, the method characterized by:
storing a plurality of frequencies including a first and a second frequency to adapt said phase lock loop;
holding voltage/current information associated with the plurality of frequencies to enable a self-calibration

in said phase lock loop when generating said plurality
of frequencies; and
in response to a trigger signal, steering an oscillator
associated with said phase lock loop from said first
frequency to said second frequency based on
voltage/current information associated with the second
frequency."

Claims 2 to 8 are dependent on claim 1. Claim 10
concerns an apparatus comprising means for performing
steps of claim 9.

VIII.   The appellant essentially argued as follows:

The decision to refuse the European patent application
mistakenly considered the following feature of claim 1
"said oscillator is configured to provide said first
frequency in response to said at least one control
signal" as being identical to a feature known from D1
(US 5 892 408 A), namely "said frequency generator
circuit is configured to provide said first frequency
in response to said at least one control signal". The
subject-matter of claim 1 was therefore not anticipated
by D1.
Further, the newly incorporated feature of "a trigger
signal that is provided to cause an update of the
digital storage from a first frequency to a second
frequency" could neither be found in document D1 nor in
any document cited in the search report. Thus any
combination of document D1 with the available prior art
would not lead to the invention.

IX.   The appellant did not comment on the preliminary
        opinion of the Board concerning the lack of novelty of
        claims 1 to 4 and 9 in view of D6 or the relevance of
        document D7.

Reasons for the Decision

1.   The appeal is admissible.

2.   *Amendments (Article 123(2) EPC)*

2.1   The following features of claim 1 of the main request
        - "input signal frequency"; and
        - "the feedback signal being produced in response to
         the output signal"
        could not be found in the original application and
        constitute an unsupported generalisation of the
        original content.

2.2   The feature "determining a change in said at least one
        control signal" (claims 1 and 9 of the main request)
        was not disclosed in the original application either.
        According to section [0021] of the published
        application "the update unit 135 ...may automatically
        determine whether one or more parameters of the PLL
        unit 120 have changed to dynamically update the pretune
        voltage" (cf. also original claims 2 and 3), and in
        response to the trigger signal the frequency generator
        sends a control signal to cause the oscillator to adapt
        the oscillator frequency (cf. e.g. section [0010]).
        There is no determination if the control signal has
        changed.

2.3   The original application did not disclose a trigger signal "to cause an update of the digital storage (140) from the first frequency to the second frequency" (claim 1 of the auxiliary request). The application as filed proposed "to dynamically update the pretune voltage" (cf. sections [0009] and [0021] and claims 3 and 6) or to "update the one or more actual valid control voltages/currents" (cf. sections [0011] and [0020] and claims 2 and 5) to "compensate for a change in one or more characteristics of the oscillator" (cf. section [0020]). "After the settling time (parameter), an actual valid (e.g., new) control voltage/current of the oscillator 150 may be converted from analog to digital and stored back into the digital storage 140 under the same address, causing the update" (cf. section [0027]). According to the original application the frequencies are not updated, only their corresponding voltage or current values are.

Claims 1 of the main and auxiliary requests and claim 9 of the main request do therefore appear to infringe Article 123(2) EPC.

3.   The expressions voltage/current or voltages/currents found in claims 1 and 9 of the main and auxiliary requests are ambiguous. An oscillator could hardly match a frequency in response to setting values being both a current and a voltage. In a usual PLL-control the desired frequencies are mapped to a voltage or a current control value but not both (cf. paragraph [0026]). The expression "voltage/current" is therefore interpreted in the following as voltage **or** current.

4.   Following this interpretation, the subject-matter of
        the independent claims of the main and auxiliary
        requests is not novel (Article 54 EPC) having regard to
        D6 which discloses:

        - a phase lock loop 10 to 20 comprising an oscillator
        14 for providing an oscillator output signal having a
        frequency based on a comparison 12 of a reference
        signal frequency f ref and a feedback signal frequency,
        the feedback signal being produced in response to the
        output signal f out (cf. figure 3);
        - the phase lock loop comprising a digital storage 26,
        28 to store information related to a plurality of
        desired frequencies, each frequency being associated
        with a voltage information held in the digital storage
        (cf. column 4, lines 22 to 25 and 34 to 45);
        - the digital storage 26, 28 together with the digital-
        to-analog converter (DAC) 22 and an operational
        amplifier 30 constituting a frequency generator in the
        sense of the frequency generator circuit 125 of the
        present application (cf. application as published,
        section [0019] and figure 1), which is capable of
        producing a control signal (cf. column 4, lines 17 to
        19 and voltage signal output of DAC 22) based on the
        first frequency and the first voltage information (cf.
        column 4, lines 20 to 25, column 5, lines 17 to 28 and
        column 6, lines 46 to 65); and
        - the oscillator being configured to provide a first
        frequency in response to the control signal;
        - the frequency generator circuit being configured to
        cause said oscillator 14 to adapt the oscillator
        frequency in response to a change in said one control
        signal (cf. sentence bridging columns 5 and 6).

The frequency adaptation continues as long as the
"error output from the phase detector 12 is at a level
greater than zero" (cf. column 5, line 62 to column 6,
line 8). In response to a negative value at the output
of detector 12 the output of operational amplifier 30
changes (Φ DET FLAG) to update the voltage information
related to said first frequency in the digital storage
(cf. column 5, lines 39 to 47 and column 6, lines 46 to
65).
The output of the amplifier 30 is a trigger signal that
enables the phase lock loop circuit of D6 to calibrate
or recalibrate the phase lock loop by pretuning the
oscillator to each frequency and updating the digital
storage (look-up table) 28 with the new voltage values
(cf. column 3, lines 13 to 30) to compensate for
problems such as aging.

The subject-matter of claims 1, 9 and 10 of the main
and auxiliary requests is therefore not new having
regard to D6.

5.   The feature of a trigger signal "provided to cause an
        update of the digital storage ... from the first
        frequency to the second frequency" is known from D6,
        where the value generated by the frequency generator 26,
        28 is incremented until the output of the operational
        amplifier 30 changes and the last value when the output
        of the amplifier 30 has changed is stored as an update
        value in the look-up table.

Order

For these reasons it is decided that:

The appeal is dismissed.

The Registrar: The Chairman:

U. Bultmann   M. Ruggiu