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Case Number: T 0540/08 - 3.4.03

Application Number: 01922058.1

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Title of invention:
Semiconductor device inspection system

Applicant:
Tokyo Electron Limited

Headword:
-

Relevant legal provisions (EPC 1973):
EPC Art. 56

Keyword:
"Inventive step (no)"

Decisions cited:
-

Catchword:
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Case Number: T 0540/08 - 3.4.03

D E C I S I O N
of the Technical Board of Appeal 3.4.03
of 5 July 2012

Appellant: (Applicant)
Tokyo Electron Limited
3-6 Akasaka 5-chome
Minato-ku
Tokyo 107-8481 (JP)

Representative:
Liesegang, Eva
Boehmert & Boehmert
Pettenkoferstraße 20-22
D-80336 München (DE)

Decision under appeal:
Decision of the Examining Division of the European Patent Office posted 8 October 2007 refusing European patent application No. 01922058.1 pursuant to Article 97(1) EPC 1973.

Composition of the Board:

Chairman: G. Eliasson
Members: R. Q. Bekkering
P. Mühlens

Summary of Facts and Submissions

I. This is an appeal against the refusal of application 01 922 058 for lack of an inventive step, Article 56 EPC 1973, over document

D1: US 5 210 041 A.

II. At oral proceedings before the board, the appellant applicant requested that the decision under appeal be set aside and a patent granted on the basis of the following:

Main request:

Claims 1 to 4 of the main request filed with the letter dated 21 May 2012;

First auxiliary request:

Claims 1 to 4 of auxiliary request I filed with the letter dated 21 May 2012;

III. Claim 1 of the main request reads as follows:

"*A probe inspection apparatus (7) for receiving a plurality of devices formed in a single substrate after completion of a manufacturing process, inspecting the devices by a probe inspection part (20) on an individual device basis, and providing an inspection result to a packaging process, the probe inspection part (20) performing an electric function test; said probe inspection apparatus (7) comprising:*

an inspection target sorting part (8) configured to omit an execution of an inspection to be applied by the probe inspection part (20) to the devices according to an inspection map created by position information gathered from the manufacturing process, which position information is supplied directly from device manufacturing apparatuses (1, 3, 5) to the probe inspection apparatus (7) and specifies positions of defective devices that have been determined to be defective in the manufacturing process, and
a marking part (18) configured to provide a mark to devices of which inspection is omitted by said inspection target sorting part (8) and to provide a mark to devices which are determined to be defective by the probe inspection part (20) thereby providing an indication that said devices provided with the mark are not to be picked up for further processing in the packaging process,
wherein the inspection target sorting part (8) includes a memory part (11) that stores the position information supplied by the manufacturing process, a map composition part (17) that creates the inspection map based on the position information stored in the memory part (11), and a central processing unit (15) for controlling the operation of the probe inspection apparatus (7)."

IV. Claim 1 of the first auxiliary request corresponds to claim 1 of the main request with the following addition (added features highlighted):

"an inspection target sorting part (8) configured to omit an execution of an inspection to be applied by the probe inspection part (20) to the devices according to

an inspection map created by position information gathered from the manufacturing process, which position information is supplied directly from **a plurality of** device manufacturing apparatuses (1, 3, 5) to the probe inspection apparatus (7)**, but not supplied from one of said plurality of device manufacturing apparatuses (1, 3, 5) to another of said plurality of device manufacturing apparatuses (1, 3,5), said information specifying** positions of defective devices that have been determined to be defective in the manufacturing process".

V. Moreover, both requests include claims directed at a device manufacturing system and a corresponding device inspection method.

VI. The appellant in substance provided the following arguments:

In document D1, the position information of the detected defective chips on a wafer was supplied to an external host computer, which in turn supplied the information to the subsequent manufacturing apparatus, prepared the control data for inhibiting the tests of the defective chips of the wafer and fed the inhibition data to the wafer-testing step. According to the invention, on the other hand, the position information of the defective chips was supplied directly from the device manufacturing apparatuses to the probe inspection apparatus thereby providing a self-sufficient system being less vulnerable and more flexible. Hence, the subject-matter of claim 1 according to the main request, as well as that of the

first auxiliary request, was both new and inventive over document D1.

Reasons for the Decision

1. The appeal is admissible.

2. *Main request*

2.1 *Novelty*

2.1.1 *Document D1*

Document 1 discloses a system comprising in the terminology of claim 1 a probe inspection apparatus for receiving a plurality of devices formed in a single substrate (wafer) after completion of a manufacturing process and inspecting the devices by a probe inspection part on an individual device basis, the probe inspection part performing an electric function test of the devices (cf column 14, line 14 to column 19, line 11; figures 1 and 5 to 12).

In particular, the system of D1 comprises an inspection target sorting part (computer 17) configured to omit an execution of an inspection to be applied by the probe inspection part (2) to the devices according to an inspection map created by position information gathered from the manufacturing process, which position information is supplied from device manufacturing apparatuses (13, 16f) to the probe inspection apparatus and specifies positions of defective devices that have been determined to be defective in the manufacturing

process (column 18, lines 1 to 12). Moreover, the inspection target sorting part (computer 17) includes a memory part (implicit) that stores the position information supplied by the manufacturing process, a map composition part (implicit) that creates the inspection map based on the position information stored in the memory part, and a central processing unit (implicit) for controlling the operation of the probe inspection apparatus.

2.1.2 As argued by the appellant, claim 1 differs from document Dl in that:

(a) the inspection result is provided to a packaging process;

(b) position information specifying defective devices is supplied directly from device manufacturing apparatuses to the probe inspection apparatus;

(c) a marking part for providing a mark to devices which are determined to be defective is provided; and

(d) the memory for storing the position information is part of the probe inspection apparatus, the inspection map is created within the probe inspection apparatus, and the inspection target sorting part of the probe inspection apparatus comprises a central processing unit for controlling the operation of the probe inspection apparatus.

Accordingly, the subject-matter of claim 1 of the main request is new over document D1 (Article 54(1) EPC 1973).

2.2 *Inventive step*

2.2.1 The above differences provide on the one hand, concerning features (a) and (c), for further processing of the devices, and on the other hand, concerning features (b) and (d), for a simplification of the set-up in that the position information of defective devices is not forwarded to successive device manufacturing apparatuses but only directly to the final probe inspection apparatus.

Accordingly, the objective problem to be solved relative to D1 is, as far as the above distinguishing features (a) and (c) are concerned, to adapt the apparatus for further processing of the devices and, as far as the above distinguishing features (b) and (d) are concerned, to simplify the apparatus where avoiding further treatment of defective devices is not required.

The above partial problems are unrelated and accordingly addressed separately.

2.2.2 Regarding the above features (a) and (c), the step of testing wafers (2) in D1 is a final testing done at completion of the wafer process 1 (cf figure 1 and corresponding description). The dice (chips) on the wafer at this point are completed with bump electrodes (CCB). Typically, probe testing is done hereafter, including marking with an ink dot or mapping the defective dice on the wafer, followed by the packaging process including dicing and packaging the individual good dice. Accordingly, as far as it is not implicit from D1 that the inspection result is provided to a

packaging process, it is at least obvious to a person skilled in the art to do so. Moreover, ink marking/mapping the defective dice at probe inspection is conventional and it is obvious in this case, as the packaging process relies on the defective dice on the wafer being marked/mapped, also to mark/map the known defective dice for which the probe inspection has been omitted.

Accordingly, for a person skilled in the art faced with the above problem of adapting the probe inspection apparatus for further processing of the devices it is obvious to include the above features (a) and (c).

2.2.3 Regarding the above features (b) and (d), the appellant argued that Dl provided a sequence of processing apparatuses in which testing data was fed forward from one processing apparatus in a chain to the next, and only those devices were processed in the subsequent step that had not been detected defective in the preceding step. This avoided the processing of defective devices and thereby allowed to minimize the processing resources and processing time. However, this advantage came at the expense of a rather complex control and information handling. Dl required a central host computer 17 for controlling the various testing steps and for passing on the control data (cf. column 15, lines 25 to 36 and column 16, lines 5 to 24). If, in the system of document Dl, the host computer were interrupted due to any kind of failure, such as a communication failure or failure in the processing, this would affect and interrupt the entire processing chain. In contrast, the invention provided for a self-sufficient testing system and method that did not rely

on control from an external computer, thus requiring less computational resources and less communication and, hence, being more flexible and less vulnerable to communication failures.

It is, however, noted that document D1 distinguishes between on the one hand the advantage brought about by the teaching of D1 that "*any spare treatment of the excessive chips or the defective chips 19a and 19b need not be performed so that the number and materials of treatments can be reduced to spare the production cost*" (column 18, points (1) to (4)) and on the other hand that "*by feeding the data of that propriety of the chips over the wafers 18b to 18d, which has been decided in the wafer process 1, forward to the wafer testing step 2, only the non-defective chips 19 over the wafers 18b to 18d may be tested at the wafer testing step 2. As a result, it is possible to shorten the testing time period of the wafer testing step 2 drastically, as compared with that of the prior art*" (column 18, point (10)).

It is obvious to a person skilled in the art that this first aspect may be dispensed with where, for instance, the wafer process is such that no treatment of individual chips is foreseen (in fact most conventional wafer processing steps such as diffusion, etching, doping etc. involve treatment of the entire wafer and do not allow for skipping treatment of individual chips) or no worthwhile cost savings are possible by skipping the treatment of individual defective chips.

Under these circumstances, as would be readily apparent to the skilled person, only the above second aspect of

shortening the testing time at final wafer test is of practical interest. In this case, it is obvious to supply the position information of the defective chips directly from each of the manufacturing apparatuses to the probe inspection apparatus used for final wafer testing.

Accordingly, it is obvious for a person skilled in the art addressing the second partial problem to include the above features (b) and (d).

The appellant argued in this respect that D1 provided a self-contained solution saving production costs and that there was nothing suggesting a skilled person to single out feeding defective device location information to the probe inspection apparatus.

It is, however, noted that in the case of a complex system as disclosed in D1, as is in fact the case in any complex system featuring a number of measures provided to address corresponding distinct issues, it is normal practice for a person skilled in the art to perform a cost/benefit analysis for each of the measures proposed and omit those measures which are not considered worthwhile or necessary. The fact that, as argued in the present case, the omission leads to an overall simplification of the system (with an ensuing increase in reliability of the system as whole) is not an effect indicative of any inventive step but rather the natural consequence of such an omission.

2.2.4 The subject-matter of claim 1 of the main request, thus, lacks an inventive step in the sense of Article 56 EPC 1973.

The above also applies, mutatis mutandis, to claim 4 directed at a corresponding device inspection method.

The appellant's main request is, therefore, not allowable.

3. *First auxiliary request*

3.1 Claim 1 of the first auxiliary request corresponds to claim 1 of the main request essentially with the addition that the position information is supplied directly from **a plurality of** device manufacturing apparatuses (1, 3, 5) to the probe inspection apparatus (7)**, but not supplied from one of said plurality of device manufacturing apparatuses (1, 3, 5) to another of said plurality of device manufacturing apparatuses (1, 3, 5)**.

3.2 These amendments do not alter the finding above for the main request, according to which it is obvious for the skilled person to supply the position information of the defective chips directly from (a plurality of) device manufacturing apparatuses to the probe inspection apparatus (and not to another device manufacturing apparatus) used for final wafer testing.

Accordingly, the subject-matter of claim 1 of the first auxiliary request also lacks an inventive step in the sense of Article 56 EPC 1973.

This also applies, mutatis mutandis, to claim 4 directed at a corresponding device inspection method.

The appellant's first auxiliary request is, therefore, not allowable either.

Order

For these reasons it is decided that:

The appeal is dismissed.

Registrar: Chair:

S. Sánchez Chiquero G. Eliasson