Internal distribution code:

(A) [-] Publication in OJ
(B) [-] To Chairmen and Members
(C) [-] To Chairmen
(D) [X] No distribution

Datasheet for the decision of 19 October 2012

Case Number: T 0239/08 - 3.5.04

Application Number: 97953233.0

Publication Number: 948792

IPC: G11C7/00, G11C7/06, G11C11/409

Language of the proceedings: EN

Title of invention:
METHOD AND APPARATUS FOR SHARING SENSE AMPLIFIERS BETWEEN MEMORY BANKS

Patentee:
Rambus Inc.

Opponent:
MICRON EUROPE Ltd

Relevant legal provisions:
EPC 1973 Art. 100(a), 100(c), 56

Keyword:
Grounds for opposition - lack of inventive step (no) - added subject-matter (no)

Decisions cited:
T0331/87

Europäisches Patentamt
European Patent Office
Office européen des brevets

Beschwerdekammern
Boards of Appeal
Chambres de recours

European Patent Office
D-80298 MUNICH
GERMANY
Tel. +49 (0) 89 2399-0
Fax +49 (0) 89 2399-4465

Case Number: T 0239/08 - 3.5.04

D E C I S I O N
of the Technical Board of Appeal 3.5.04
of 19 October 2012

Appellant: (Opponent)	MICRON EUROPE Ltd Micron House Wellington Business Park Dukes Ride Crowthorne Berkshire RG45 6LS (GB)
Representative:	Tunstall, Christopher Stephen Carpmaels & Ransford One Southampton Row London WC1B 5HA (GB)
Respondent: (Patent Proprietor)	Rambus Inc. 1050 Enterprise Way, Suite 700 Sunnyvale, CA 94089 (US)
Representative:	Eisenführ, Speiser & Partner Johannes-Brahms-Platz 1 20355 Hamburg (DE)
Decision under appeal:	**Interlocutory decision of the Opposition Division of the European Patent Office posted 30 November 2007 concerning maintenance of the European Patent No. 948792 in amended form.**

Composition of the Board:

Chairman: F. Edlinger
Members: A. Dumont
T. Karamanli

Summary of Facts and Submissions

I. The patent proprietor appealed against the decision by the opposition division maintaining European patent No. 0 948 792 in amended form on the basis of the then first auxiliary request which differed only in claim 7 from claims 1 to 11 as granted.

II. An opposition had been filed requesting revocation of the patent in its entirety on the grounds for opposition pursuant to Article 100(a), (b) and (c) EPC 1973 (lack of inventive step, added subject-matter and insufficient disclosure of the invention according to claim 7 as granted, respectively).

III. The opponent appealed against the decision to maintain the patent in amended form and requested that the patent be revoked, on the grounds of lack of inventive step and added subject-matter (Articles 100(a) and (c) EPC 1973, respectively).

IV. The appellant replied and requested that the appeal be dismissed.

V. The following prior-art documents were referred to:

D1: JIN-MAN HAN et al.: "Skew Minimization Techniques for 256M-bit Synchronous DRAM and beyond", 1996 Symposium on VLSI Circuits Digest of Technical Papers;
D2: US 5,267,214 A;
D3: US 5,251,176 A;
D4: US 5,586,078 A;
D5: US 5,596,521 A; and
D6: US 5,384,745 A.

VI. In an annex to the summons to oral proceedings, the board observed *inter alia* that the interpretation of the last feature of the preamble of claim 1 (sense amplifier/s "coupled to") seemed of significance for the question of whether claim 18 as originally filed could be considered as a basis for claim 1 and whether the omission of a feature of original claim 18 relating to the determination of a memory bank associated with a requested address constituted an unallowable amendment. The board also made observations on the different prior art documents.

VII. Neither party commented on the board's observations in the annex to the summons, but they both announced in writing that they would not be attending oral proceedings. Thus the oral proceedings took place on 19 October 2012 in their absence.

VIII. Claim 1 reads as follows:

"A memory device comprising:
a first memory bank (BANK0) including at least one subarray (62a) of memory cells, the first memory bank having a first row decoder (64) and a first column decoder (76);
a second memory bank (BANK1) including at least one subarray (80) of memory cells, the second memory bank having a second row decoder and a second column decoder (78);
a first plurality of sense amplifiers including at least one sense amplifier (70) coupled to one memory subarray (62a) in the first memory bank and coupled to one memory subarray (80) in the second memory bank

characterised in that

a control mechanism is configured to determine whether the sense amplifier (70) is already in use; and access the data if the sense amplifier (70) is not already in use to avoid simultaneous access to memory subarrays that share the sense amplifier (70)."

IX. Claim 9 reads as follows:

"A method for accessing data stored in a memory device, wherein the memory device includes at least two memory banks that share at least one sense amplifier (70), the method comprising the steps of:
(a) receiving a request to access a particular address; and
(b) determining a memory bank associated with the requested address;

characterized by the steps of

(c) determining whether the sense amplifier (70) associated with the memory bank determined in step (b) is already in use; and
(d) accessing the data associated with the requested address if the sense amplifier (70) associated with the memory bank determined in step (b) is not already in use."

X. As regards added subject-matter, the reasoning in the decision under appeal may be summarised as follows:

Originally-filed claim 18 forms the basis of claim 1. It recites a step of "accessing the data ... if sense amplifiers associated with the memory bank ... are not already in use". It is thus necessary to check whether all sense amplifiers associated with the selected memory bank are available for use, before accessing

data (see also figure 6 and page 11, lines 28 to 31 in the application). Claim 1 does not include the availability check of the other associated sense amplifiers and the condition that the other associated sense amplifiers are available.

No other interpretation of claim 1 is possible than relating "the sense amplifier (70)" of the characterising portion of claim 1 with the shared "at least one sense amplifier (70)" in the preamble, in the light of the description and in order to solve the technical problem posed.

The goal of the invention is to prevent simultaneous access to memory banks sharing sense amplifiers. Hence, checking the availability of the shared sense amplifiers between the two memory banks is sufficient, because the other sense amplifiers of the selected memory bank are not shared and hence are available for use. Checking the availability of other, non-shared, sense amplifiers was never explained as essential in the original disclosure. Furthermore, the removal of this latter check requires no modification of other features. The three-step test according to the Guidelines for Examination, C-VI, 5.3.10, is thus successful.

Furthermore, both original claim 18 and present claim 1 focus on a memory device comprising two memory banks and at least one shared sense amplifier between the two banks. Claim 1 does not mention a third memory bank, with one sense amplifier shared between the second and third memory banks, so that an additional check of this shared sense amplifier is not necessary to access the second memory bank.

Consequently, the amendments in claim 1 (and the corresponding method claim 9) do not extend beyond the content of the application as filed.

XI. As regards added subject-matter, the appellant essentially argued as follows:

Claim 1 is not limited to a device with only two memory banks, although it does not expressly mention a third bank. Sense amplifiers not shared between two subarrays in the two banks are also not specified. For example, claim 1 does not preclude one or more of these remaining sense amplifiers from being shared between one (BANK1) of the two banks recited in claim 1 and a third bank (BANK2 in figure 4). According to claim 1, if the shared sense amplifier (70) is not in use, then the first memory bank is accessed. A further check of the at least one sense amplifier (82) shared with the third bank is however described as necessary prior to accessing the second bank. The result is that the embodiment of figure 4 of the patent in suit is not excluded by the wording of claim 1, but that the reduced functionality of claim 1 is not supported for that embodiment.

By contrast, claim 18 of the application as originally filed, on which present claim 1 is based, determines whether all sense amplifiers associated with the memory bank in question are not in use before allowing access to requested data. So, claim 18 also prevents simultaneous access to memory subarrays that share more than one sense amplifier such as in the embodiment of figure 4. This shows that the scope of claim 18 has been broadened during the examining proceedings, adding fresh subject-matter.

A positive answer to any one of the questions in the three-step test formulated in decision T 331/87 results in the finding of added subject-matter. In the present case, claim 1 fails the first step of the test, because the features removed were explained as essential.

XII. As regards added subject-matter, the respondent's arguments additional to those in the decision under appeal may be summarised as follows:

The embodiments of figures 2 and 4 in the patent in suit avoid simultaneous access to memory subarrays which share at least one sense amplifier of the plurality of sense amplifiers if the at least one shared sense amplifier is already in use by another memory subarray. It is irrelevant whether the memory subarrays are coupled to another plurality of sense amplifiers within the same memory bank (embodiment of figure 2) or also to another plurality of sense amplifiers of another memory bank (embodiment of figure 4).

Features such as further pluralities of sense amplifiers not shared between the banks (embodiment of figure 2) or further pluralities of sense amplifiers shared by different adjacent banks (embodiment of figure 4) are neither required nor excluded by claim 1 as filed or as maintained, or by any other claims as filed or as maintained. Moreover, such features are completely irrelevant to the present invention, since to implement the present invention it is sufficient to consider just the at least one shared sense amplifier of the plurality of sense amplifiers and the two memory subarrays of the two memory banks which are both coupled to the at least one shared sense amplifier.

The appellant's assumptions are purely hypothetical in that they are based on scenarios which are not excluded by the wording of claim 1, or on facts and features which are not included and expressed by the wording of the patent in suit. Furthermore, according to claim 1, the whole "first plurality of sense amplifiers" is shared, not just the "at least one sense amplifier (70)". There are no remaining sense amplifiers which could be coupled to a third memory bank.

XIII. As regards inventive step, the reasoning in the decision under appeal may be summarised as follows:

D1 discloses a device according to the preamble of claim 1, in particular with one of the amplifiers (IO S/A) being the shared "at least one sense amplifier" of claim 1. D2 discloses a mechanism controlling the connection between sense amplifiers and memory blocks but does not disclose a mechanism determining whether sense amplifiers are already in use. None of the available prior-art documents discloses a control mechanism configured to determine whether the at least one shared sense amplifier is in use and to access the data if the at least one shared sense amplifier is not already in use, as defined in claim 1.

The person skilled in the art would only have provided sequential access to the memory banks sharing the same sense amplifier. Furthermore, the opponent's examples based on every-day behaviour of people sharing an object reflect an *ex post facto* analysis, in selecting one of a plurality of alternatives: two persons could agree to use a shared object at different times instead of checking the availability of the shared object. Moreover, every-day behaviour cannot be applied

directly to the field of memory banks without exercising an inventive step. Thus the subject-matter of claim 1 is inventive.

XIV. As regards inventive step, the appellant essentially argued as follows:

The subject-matter of claim 1 lacks an inventive step in view of the teaching of D1 at least. Figure 1 of D1 discloses a memory device, in particular with input/ output sense amplifiers shared between two adjacent memory banks. Such amplifiers differ from bit line sense amplifiers described in the patent in suit. The definition of the sense amplifiers in claim 1 is however a general one.

The problem of minimising die area and thus cost is solved by sharing sense amplifiers between memory banks within a memory device. It was known at the priority date of the patent in suit to share sense amplifiers, and thus to save die space and cost, on an inter-memory (bank) level as well as on an intra-memory (subarray) level. Furthermore, D1 inherently discloses a control mechanism but is silent regarding its operation. The objective technical problem to be solved with regard to the closest prior-art document D1 is therefore how to configure the control mechanism to avoid simultaneous access to memory subarrays that share the sense amplifier.

It was well known that banks in a multiple-bank memory device were independent and that each memory bank within a memory device was capable of being operated and accessed simultaneously and separately from the other memory banks in the device. This is shown in D6 and also acknowledged in the patent in suit.

The memory device of D1 is such a multiple-bank memory device, with memory banks which can be accessed simultaneously. When multiple memory access requests are received simultaneously by the memory controller, these requests include access requests for adjacent banks that share sense amplifiers.

It was well known in the art that collisions in the use of shared sense amplifiers were to be avoided by controlling the shared sense amplifiers such that they are connected to only one of the blocks of memory between which they are shared when memory access utilising that shared sense amplifier is under way. This is exemplified in D2, which discloses a memory device split into memory blocks, with bit-line sense amplifiers shared between adjacent blocks. Sense amplifier control signals are generated by a circuit (figure 10 and the associated description) to connect the shared sense amplifiers to one block and to disconnect them from the other blocks to which they may be connected. Thus the sense amplifiers are controlled to avoid simultaneous access to the blocks to which they are connected. This form of control is also exemplified in D3 and D4. Another example of sense amplifiers being shared between memory banks in a memory device may be found in figure 7 of D5, which is prior art for the reason that the earliest priority is not validly claimed in the patent in suit.

Obviousness is also demonstrated as follows. The immediate reaction of any person presented with the objective technical problem of how to avoid simultaneous use by multiple users of a shared item is to have a prospective check as to whether the shared item is already being used before commencing use, and

to commence use only if the shared item is not in use by another user. Various examples of this "every-day life behaviour" exist. One such example is the sharing of a PC by two research students in a university. Another example is the sharing, between two or more people, of a portable disc drive for a PC or laptop computer. This behaviour is routine and transferable across technical fields, and the skilled person is no different to any other person in this respect.

For these reasons, claim 1 is not inventive.

XV. As regards inventive step, the respondent stated that the analysis in the decision under appeal was correct and referred to the arguments presented in the opposition proceedings.

Reasons for the Decision

1. The appeal is admissible.

2. Article 83 EPC 1973

The opposition division decided that the ground for opposition under Article 100(b) EPC 1973 raised against claim 7 as granted prejudiced the maintenance of the patent unamended. This objection was not raised against amended claim 7 according to the auxiliary request, on which the patent as maintained in amended form was based, either in the opposition proceedings or in the statement of grounds of appeal. The board too sees no reason to raise sufficiency of disclosure under Article 83 EPC 1973 as an issue.

3. Article 100(c) EPC 1973

3.1 "[T]he sense amplifier (70)" of the characterising portion of claim 1 refers back to the (shared) "at least one sense amplifier (70)" of the preamble. This means that the control mechanism carries out the determination for all sense amplifiers coupled between the subarrays (62a, 80) of a first and a second memory bank (BANK0, BANK1) as defined in the preamble. This interpretation is not contested by the appellant.

3.2 The respondent relates the participle "coupled" to the whole "first plurality of sense amplifiers" in the last feature of the preamble of claim 1 and thus interprets it as "a first plurality of sense amplifiers coupled to one memory subarray (62a) in the first memory bank and coupled to one memory subarray (80) in the second memory bank, the first plurality including at least one sense amplifier (70)". This would mean that all sense amplifiers in the first plurality are coupled to the two memory subarrays (62a, 80), leaving no remaining sense amplifiers that would not be subject to the control mechanism defined in the characterising portion.

3.3 By contrast, the board adopts a more general interpretation of claim 1, where only the "at least one sense amplifier (70)" has to be coupled to the two memory subarrays (62a, 80). Thus some sense amplifiers in the "first plurality" might not be subject to the control mechanism. These (possibly remaining) sense amplifiers would be coupled differently from the "at least one sense amplifier (70)". They could for instance be shared with another (third) memory bank (BANK2 in figure 4) or shared between memory subarrays within a single bank (such as sense amplifier 26b in figure 2).

3.4 Claim 1 does not define explicitly a further (third) memory bank, with shared sense amplifiers which might cause malfunction in the case of simultaneous access to different memory banks, which is at the heart of the present invention. Rather, claim 1 defines (and thus focuses on) the control mechanism for avoiding malfunction in the case of sense amplifier(s) shared between two memory banks. The board judges that claim 1 defines a control mechanism with all the steps necessary to avoid collision in this very case, by avoiding simultaneous use of (all) the sense amplifiers shared between these two banks and which are referred to as "at least one sense amplifier". The appellant has not argued to the contrary.

3.5 Claim 1 is not limited to a device with only two memory banks. The board agrees that implementing the control mechanism of claim 1 in a memory device with sense amplifiers shared with a further (third) memory bank would require further measures to avoid simultaneous access. However, claim 1 does not define technical features of the memory device, such as a third memory bank and its shared sense amplifiers, which would require further measures in the control mechanism. The definitions in claim 1 are thus sufficient to avoid simultaneous access of the sense amplifiers under consideration (the "at least one sense amplifier").

3.6 Claim 18 as originally filed relates to a method for accessing data stored in a memory device including "at least two memory banks that share at least one sense amplifier". The features of claim 18 omitted in the appellant's view relate to determining whether all sense amplifiers associated with the memory bank in question (associated with a requested address) are not

in use before allowing access to requested data. In the board's interpretation, the control mechanism of claim 18 involves only the sense amplifier(s) shared between the two memory banks. It involves neither further sense amplifiers which would be shared with a hypothetical further (third) memory bank, nor the step of checking the use of all sense amplifiers associated with the memory bank (associated with a requested address).

3.7 Thus neither present claim 1 nor claim 18 as originally filed contains concrete technical features of a control mechanism which would involve sense amplifiers shared between one memory bank (such as BANK1 in figure 4) and two adjacent memory banks (such as BANK0 and BANK2 in figure 4). As a result, the board considers that no such features have been removed from claim 18 or replaced, so that the three-step test developed in decision T 331/87 (OJ EPO 1991, 22), or as set out in the Guidelines for Examination (H-V, 3.1, previously C-VI, 5.3.10) cannot lead to the conclusion that a feature which was explained as essential has been removed.

3.8 It results from the above that the appellant has not convinced the board that the patent as maintained in amended form by the opposition division contains added subject-matter in claim 1. Thus the ground for opposition under Article 100(c) EPC 1973 must fail.

4. Article 100(a) in combination with Article 56 EPC 1973

4.1 D1 was regarded as the closest prior-art document by the appellant and by the opposition division. D1, in particular figure 1 thereof, discloses a memory device comprising the features set out in the preamble of

claim 1, in the case covered by the claim where each bank includes one subarray. Sense amplifiers (IO S/A) are shared between adjacent banks (BANK0, BANK1). As acknowledged by the appellant, D1 discloses a memory architecture but is silent about any control mechanism for accessing the memory banks. The appellant assumes that the device of D1 allows two addresses to be simultaneously processed, which would possibly cause simultaneous access requests to two adjacent banks sharing sense amplifiers. However, in the board's view, this assumption is not justified by the paragraph of D1 relating to the device architecture or by figure 1, or by any other passage of D1.

As a result, the control mechanism defined in the characterising portion of claim 1, addressing problems arising from possible simultaneous access to adjacent banks, is not known from D1.

4.2 Including, in the objective technical problem solved over D1, the aspect of simultaneous access would be tantamount to introducing an element reaching beyond the teaching of D1 and thus hinting to some extent at the solution. Thus the board considers that the objective technical problem should be generally formulated as providing in memory devices of the kind disclosed in D1 an appropriate control mechanism for accessing banks sharing at least one sense amplifier.

4.3 This problem is solved according the present invention with a control mechanism implementing steps relating to the control of the memory device in the event of simultaneous access to the memory (see also paragraph [0004] in the patent in suit).

4.4 The appellant cites prior-art documents disclosing memory devices with shared sense amplifiers. More specifically:

- D2 discloses a memory device divided into memory blocks and comprising a circuit (figure 10) for generating signals (SA, SB, SC, SD) controlling shared sense amplifiers, where only one of the block designating signals (X1 to X4) may be active at a time (see for instance column 3, lines 26 to 29 and column 16, lines 22 to 24). This prevents two adjacent blocks from being simultaneously connected to the shared sense amplifiers.

- D3 discloses a memory device divided into memory blocks, where only the block related to an applied address is selected, in order to reduce power consumption (see column 8, lines 18 to 24).

- D4 distinguishes between independent sense amplifiers, which could be operated simultaneously, and sense amplifiers shared between subarrays, which have to be used "time-divisionally" (see column 2, line 65 to column 3, line 28).

Thus documents D2 to D4 teach that two memory blocks, for instance two subarrays, may not simultaneously use a common, shared, sense amplifier, and that access should then take place sequentially.

Moreover, D6 (column 19, lines 37 to 50 and column 23, lines 17 to 22) as well as the prior art cited in the patent in suit (see paragraphs [0004] and [0010] thereof) associate simultaneous access with separate (i.e. unshared, independent) sense amplifiers.

None of this prior art suggests associating simultaneous access (or simultaneous attempts to access) with memory blocks sharing sense amplifiers, either on an inter-memory ("bank") level or on an intra-memory ("subarray") level.

4.5 In conclusion, a control mechanism assuming simultaneous access is not disclosed in the device of D1. Furthermore, a mechanism associating simultaneous access and shared amplifiers is not suggested in the further prior art cited. The board is thus not convinced that the provision of the control mechanism of claim 1, which only makes sense in a device allowing simultaneous access, would be obvious without adopting an impermissible *ex post facto* approach. The analogy with "every-day life behaviour" mentioned by the appellant would also require hindsight and it is also not convincing.

4.6 Document D5 would be comprised in the state of the art within the meaning of Article 54(2) EPC 1973 only if the earliest priority of the present application were not validly claimed. As argued by the appellant, D5 illustrates "[a]nother example of sense amplifiers being shared between memory banks in a memory device". D5 is thus not more relevant for assessing inventive step than documents D2 to D4. Consequently the validity of the earliest priority claim of the patent in suit is not decisive and need not be examined.

4.7 In conclusion, the appellant has not convinced the board that the subject-matter of claim 1 was obvious having regard to the prior art cited. Thus the subject-matter of claim 1 is inventive (Article 56 EPC 1973)

and the ground for opposition under Article 100(a) EPC 1973 must fail.

5. Independent method claim 9 corresponds in substance to device claim 1, in particular as regards the determining and accessing steps (which the control mechanism of claim 1 is configured to carry out). As a result, the board's conclusions regarding inventive step and added subject-matter with regard to claim 1 apply equally to claim 9.

6. In conclusion, none of the grounds for opposition precludes maintenance of the European patent in amended form.

Order

For these reasons it is decided that:

The appeal is dismissed.

The Registrar: The Chairman:

K. Boelicke F. Edlinger

Decision electronically authenticated