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Datasheet for the decision of 25 January 2011

Case Number: T 0108/08 - 3.4.03

Application Number: 00102398.5

Publication Number: 1033759

IPC: H01L 29/78

Language of the proceedings: EN

Title of invention:
MOS-gated device having a buried gate and process for forming same

Patentee:
Fairchild Semiconductor Corporation

Opponent:
-

Headword:
-

Relevant legal provisions:
-

Relevant legal provisions (EPC 1973):
EPC Art. 56

Keyword:
"Inventive step (yes)"

Decisions cited:
-

Catchword:
-

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Case Number: T 0108/08 - 3.4.03

D E C I S I O N
of the Technical Board of Appeal 3.4.03
of 25 January 2011

Appellant: Fairchild Semiconductor Corporation
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Representative: Liesegang, Eva
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Decision under appeal: **Decision of the Examining Division of the European Patent Office posted 13 August 2007 refusing European patent application No. 00102398.5 pursuant to Article 97(1) EPC 1973.**

Composition of the Board:

Chairman: G. Eliasson
Members: T. Häusser
T. Bokor

Summary of Facts and Submissions

I. The appeal concerns the decision of the examining division refusing European patent application No. 00 102 398 for lack of inventive step (main request and first to fourth auxiliary request) having regard to the following documents:

D1: PATENT ABSTRACTS OF JAPAN vol. 014, no. 391 (E-0968), 23 August 1990 & JP 2-144971 A

D2: MATSUMOTO S ET AL: "A HIGH-PERFORMANCE SELF-ALIGNED UMOSFET WITH A VERTICAL TRENCH CONTACT STRUCTURE" IEEE TRANSACTIONS ON ELECTRON DEVICES, vol. 41, no. 5, May 1994, pages 814-818, NEW YORK, NY, USA

D3: BULUCEA C ET AL: "TRENCH DMOS TRANSISTOR TECHNOLOGY FOR HIGH-CURRENT (100 A RANGE) SWITCHING" SOLID STATE ELECTRONICS, vol. 34, no. 5, May 1991, pages 493-507

II. The following documents are also referred to in this decision:

D1a: translation of JP 2941823 B (patent specification corresponding to D1)

III. At the oral proceedings before the board the appellant requested that the decision under appeal be set aside and that a patent be granted in the following version:

Description: 1, 1a, 2, 3 as filed during the oral proceedings

	4-7	as originally filed
Claims:	1-12	as filed with the grounds of appeal (as Main Request)
Drawings:	Figures 1, 2A-D, 3A-C (Sheets 1-5)	as originally filed.

IV. The wording of the independent claims 1 and 6 reads as follows:

"1. A trench MOS-gated device comprising a substrate (201; 301) comprising doped monocrystalline semiconductor material, a doped upper layer (202; 302) disposed on said substrate, said upper layer (202; 302) having an upper surface and comprising at said upper surface a plurality of heavily doped body regions (204; 304) having a first polarity, said upper layer (202; 302) further comprising at said upper surface a plurality of heavily doped source regions (206; 306) having a second polarity and extending from said upper surface to a selected depth in said upper layer (202; 302), said upper layer further comprising a well region (205; 305) having said first polarity, said well region (205; 305) underlying said body and source regions (204, 206; 304, 306) and lying above a drain region (203; 303) in said upper layer (202; 302), a gate trench (207; 307) separating one of said source regions (206; 306) from a second source region (206; 306), said trench (207; 307) extending from said upper surface of said upper layer (202; 302) to said drain region (203; 303), said trench having a floor (209; 309) and sidewalls (208; 308) comprising a layer of dielectric material (212; 312), said trench (207; 307) being filled with a conductive gate material (210; 310) to a

selected level substantially below the upper surface of the upper layer (202; 302) and with an isolation layer of dielectric material (212; 312) overlying said gate material (210; 310), wherein said selected level is sufficiently low such as to permit the inclusion of said dielectric material (212; 312) in the trench of sufficient thickness to provide gate insulation, said overlying layer of dielectric material (212; 312) in said trench (207; 307) having an upper surface that is coplanar with or slightly below said upper surface of said upper layer (202; 302), in which the substrate (201; 301) comprises monocrystalline silicon, and upper layer (202; 302) comprises an epitaxial layer."

"6. A process for forming a trench MOS-gated device, said process comprising:
(a) forming a doped upper layer (202; 302) on a semiconductor substrate (201; 301), said upper layer (202; 302) having an upper surface and an underlying drain region (203; 303),
(b) forming a well region (205; 305) having a first polarity in said upper layer (202; 302), said well region (205; 305) overlying said drain region (203; 303);
(c) forming a gate trench mask (TM) on said upper surface of said upper layer (202; 302);
(d) forming a plurality of gate trenches (207; 307) extending from the upper surface of said upper layer (202; 302) through said well region (205; 305) to said drain region (203; 303);
(e) forming sidewalls (208; 308) and floor (209; 309) each comprising a dielectric material (212; 312) in each of said gate trenches (207; 307);

(f) filling each of said gate trenches (207; 307) to a selected level substantially below the upper surface (202; 302) of said upper level with a conductive gate material (210; 310); wherein said selected level is sufficiently low such as to permit inclusion of dielectric material (212; 312) in the trench of sufficient thickness to provide gate insulation
(g) removing said trench mask (TM) from the upper surface of said upper layer (202; 302);
(h) forming an isolation layer of dielectric material (212; 312) on the upper surface of said upper layer (202; 302) and within said gate trench (207; 307), said isolation layer overlying said gate material (210; 310) and substantially filling said trench (207; 307);
(i) removing said dielectric layer from the upper surface of said upper layer (202; 302), said dielectric layer remaining within and substantially filling said trench (207; 307) having an upper surface that is coplanar with or slightly below the upper surface of said upper layer (202; 302);
(j) after forming the trench (207; 307), forming a plurality of heavily doped source regions (206; 306) having a second polarity in said body regions (204; 304), said source regions (206; 306) extending to a selected depth from the upper surface of said upper layer (202; 302) to overlap the conductive gate material (210; 310) in the trench;
(k) forming a plurality of heavily doped body regions (204, 206; 304, 306) having a first polarity at the upper surface of said upper layer (202; 302), said body regions (204, 206; 304, 306) overlying the drain region (203; 303) in said upper layer and terminating inside the well region (205; 305); and

(l) forming a metal contact (215; 315) to said body and source regions (205, 206; 305, 306) over the upper surface of said upper layer (202; 302)."

V. The appellant argued essentially as follows:

Document D1 disclosed a high concentration region 13, a base region 3 and drain area 2, which corresponded to the heavily doped body region, the well region, and the drain region of claim 1, respectively. The aim of the device of document D1 was to suppress any parasitic bipolar transistor operation. This was achieved by providing a deep high concentration region 13, which traversed the base region 3 and reached the drain area 2. D1 could therefore not be regarded as a realistic starting point for developing the claimed method or device, in which the well region was underlying the body region, so that the body region did not reach the drain region.

Furthermore, it was an important aspect of the manufacture in D1 to form the deep high concentration region 13 first, as the high temperature and long exposure time needed would otherwise affect all the other formed layers. D1 is thus not a promising springboard for developing the claimed method, in which the body region is formed later.

The closest state of the art was thus regarded to be the surface contact U-grooved MOSFET (SC-UMOS) disclosed in document D2.

The objective technical problem was to reduce the on-resistance characteristics as can be derived from

the description, page 4, lines 32-33, and page 6, lines 2-4.

Document D2 already disclosed a solution to the problem by providing the trench contact U-grooved MOSFET (TC-UMOS), which had reduced on-resistance characteristics as shown in Figure 4. The skilled person would thus be led to the TC-UMOS if he wanted to reduce the on-resistance, rather than to modify the SC-UMOS. The claimed invention therefore involved an inventive step.

Reasons for the Decision

1. Admissibility

The appeal is admissible.

2. Amendments

Claim 1 is based on claims 1 and 2 as originally filed and on the description as originally filed (page 5, lines 14 to 16; page 6, lines 1 to 4). Claim 6 is based on claim 7 as originally filed and on the description and drawings as originally filed (page 5, lines 14 to 16; page 6, lines 1 to 8; Figures 2A, 2B, and 2C).

Dependent claims 2 to 5 and 7 to 11 are based on original claims 3 to 6 and 9 to 13, respectively. Dependent claim 12 is based on claim 1 as originally filed. The description has been brought into conformity with the amended claims and supplemented with an indication of the relevant content of the prior art.

Accordingly, the board is satisfied that the amendments comply with the requirements of Article 123(2) EPC.

3. Novelty

3.1 Document D1

3.1.1 Document D1 discloses (see the description of Figures 1 and 2 in the translation D1a of the corresponding patent specification) a metal-oxide semiconductor field effect transistor comprising an n-type high concentration semiconductor substrate 1 on which is formed an n-type epitaxial layer as a drain area 2, a p-type base region 3, and an n-type source region 4. A recess contains a silicon oxide gate dielectric film 5, polycrystalline silicon as a gate electrode 6, and a silicon oxide layer 9 covering the gate electrode 6. Furthermore, document D1 discloses a p-type high concentration region 13. The structure is covered on the top and bottom sides by a source electrode 7 and a drain electrode 8, respectively.

3.1.2 In the wording of claim 1, document D1 discloses a trench MOS-gated device comprising a substrate (1) comprising doped monocrystalline semiconductor material (since the drain area 2 is *epitaxial*), a doped upper layer disposed on said substrate, said upper layer having an upper surface and comprising at said upper surface a plurality of heavily doped body regions (13) having a first polarity (regions on either side of the gate electrode 6), said upper layer further comprising at said upper surface a plurality of heavily doped source regions (4) having a second polarity (regions on

either side of the gate electrode 6) and extending from said upper surface to a selected depth in said upper layer, said upper layer further comprising a well region (3) having said first polarity and lying above a drain region (2) in said upper layer (see Figure 1, reference signs 2 and 3), a gate trench (the recess containing the gate electrode 6) separating one of said source regions (4) from a second source region (4), said trench extending from said upper surface of said upper layer to said drain region (2) (see Figure 1, reference signs 2, 5, and 6), said trench having a floor and sidewalls comprising a layer of dielectric material (5), said trench being filled with a conductive gate material (6) to a selected level substantially below the upper surface of the upper layer and with an isolation layer of dielectric material (9) overlying said gate material (6), wherein said selected level is sufficiently low such as to permit the inclusion of said dielectric material (9) in the trench of sufficient thickness to provide gate insulation (since the layer 9 is insulating), in which the substrate (1) comprises monocrystalline silicon, and upper layer comprises an epitaxial layer (2).

3.1.3 Document D1 also discloses (see Figure 2, reference signs 2 and 13, and the corresponding description in D1a) that the high concentration region 13 traverses the base region 3 and reaches the drain area 2 in order to improve the tolerance when switching large inductive loads. Therefore, document D1 does not disclose the following feature of claim 1:

– said well region underlying said body region.

Furthermore, the silicon oxide layer 9 covering the gate electrode 6 is formed by thermal oxidation of the polycrystalline silicon used for the gate electrode (see Figure 2(f) and (g) and the corresponding description in D1a). If the Figures gave accurate representations of the shapes of the layers of the device, such oxidation would be expected to propagate not only into the polycrystalline silicon of the gate electrode 6 but also into the source region 4. This is however not shown in the Figures, which are therefore considered to provide merely rough drafts of these shapes. Furthermore, in D1 there is no disclosure of a planarization step of the silicon oxide layer (see the corresponding document D1a). Since the thermal oxidation leads to the well-known bulging up of the silicon oxide, shown for example in Figure 2(d) of document D2, the board is therefore of the opinion that the following feature can neither be derived from the description nor from the Figures and thus does not form part of the disclosure of D1:

– said overlying layer of dielectric material in said trench having an upper surface that is coplanar with or slightly below said upper surface of said upper layer.

3.1.4 Similarly, document D1 does not disclose the following features of claim 6:

– removing said dielectric layer from the upper surface of said upper layer, said dielectric layer remaining within and substantially filling said trench having an upper surface that is coplanar with or slightly below the upper surface of said upper layer;

– forming a plurality of heavily doped body regions having a first polarity at the upper surface of said upper layer, said body regions overlying the drain region in said upper layer and terminating inside the well region.

3.1.5 The subject-matter of claims 1 and 6 is therefore new over document D1.

3.2 Document D2

3.2.1 Document D2 discloses (see Figures 1 and 2 and parts II. and III. of the description) U-grooved MOSFET's (UMOS) having an n-type silicon layer with (100) orientation, an n-type epitaxial buffer layer, p-type body regions, and n^+-type source regions. The U-groves have a silicon dioxide layer grown on the walls and are filled with poly-silicon as a gate electrode, which is oxidized at the top surface to form silicon dioxide. On the back side of the device a drain electrode is deposited.

The top contacts are either arranged in trenches or on the surface leading to a trench contact UMOS (TC-UMOS; Figure 1(a)) or a surface contact UMOS (SC-UMOS; Figure 1(b)), respectively.

The TC-UMOS has the contact trenches penetrating the source regions and reaching the body regions. The trenches have boron ions implanted on the bottom to form p^+-type regions (Figure 1(a), "p^+") and are filled with tungsten. An aluminium layer defines the source and drain electrodes.

The SC-UMOS also has p^+-type regions (Figure 1(b), "p^+") and furthermore an aluminium-silicon layer defines source and gate electrodes. The purpose of the p^+-type regions is to improve the contact characteristics between the electrode and the body regions by avoiding the formation of a Schottky barrier (see the reference "Body Contact" in Figure 1(b)). The p^+-type regions can therefore be assumed to be in contact with the p-type body regions.

3.2.2 The SC-UMOS is closer to the subject-matter of claim 1 than the TC-UMOS and comprises in the wording of claim 1 a trench MOS-gated device (UMOS) comprising a substrate comprising doped monocrystalline semiconductor material (n-type silicon layer with (100) orientation), a doped upper layer disposed on said substrate, said upper layer having an upper surface and comprising at said upper surface a plurality of heavily doped body regions having a first polarity (p^+ regions), said upper layer further comprising at said upper surface a plurality of heavily doped source regions having a second polarity and extending from said upper surface to a selected depth in said upper layer (n^+ source regions), said upper layer further comprising a well region having said first polarity (body regions), said well region underlying said body and source regions (Figure 1(b), "Body", "Source", "p^+") and lying above a drain region (n-type epitaxial buffer layer) in said upper layer, a gate trench (U-groove) separating one of said source regions from a second source region (Figure 1(b), "Source", U-groove filled with "poly-Si"), said trench extending from said upper surface of said upper layer to said drain region (Figure 1(b), "n^-", U-groove filled with "poly-Si"), said trench having a

floor and sidewalls comprising a layer of dielectric material (silicon dioxide layer), said trench being filled with a conductive gate material (poly-silicon) to a selected level substantially below the upper surface of the upper layer and with an isolation layer of dielectric material (silicon dioxide layer) overlying said gate material (poly-silicon), wherein said selected level is sufficiently low such as to permit the inclusion of said dielectric material in the trench of sufficient thickness to provide gate insulation (since the silicon dioxide layer is insulating), in which the substrate comprises monocrystalline silicon (silicon layer with (100) orientation), and upper layer comprises an epitaxial layer (epitaxial buffer layer).

The oxidation of the poly-silicon gate electrode - described in document D2 - which results in the silicon dioxide layer covering the gate electrode, leads to a bulging up of that silicon dioxide layer. This is also shown in Figures 1(b) and 2(d) ("SiO_2"). Therefore, the top surface of the n^+-type source regions is at a lower level than the top surface of the silicon dioxide layer covering the gate electrode.

Hence, document D2 does not disclose the following feature of claim 1:

– said overlying layer of dielectric material in said trench having an upper surface that is coplanar with or slightly below said upper surface of said upper layer.

3.2.3 Similarly, document D2 does not disclose the following feature of claim 6:

– removing said dielectric layer from the upper surface of said upper layer, said dielectric layer remaining within and substantially filling said trench having an upper surface that is coplanar with or slightly below the upper surface of said upper layer.

3.2.4 The subject-matter of claims 1 and 6 is therefore new over document D2.

3.3 The remaining prior art documents on file are not closer to the subject-matter of claims 1 and 6 than documents D1 and D2. Claims 2 to 5 and 7 to 12 are dependent on claims 1 and 6, respectively, providing further limitations.

Accordingly, the subject-matter of claims 1 to 12 is new (Article 52(1) EPC and Article 54(1), (2) EPC 1973).

4. Inventive step

4.1 The SC-UMOS disclosed in document D2 (Figure 1(b)) is regarded to be structurally closest to the subject-matter of claim 1 and is therefore regarded to be the closest state of the art.

4.2 The subject-matter of claim 1 differs from the SC-UMOS disclosed in document D2 in comprising the following features (see point 3.2 above):

(i) said overlying layer of dielectric material in said trench having an upper surface that is coplanar with or slightly below said upper surface of said upper layer.

4.3 The effect of these features is to increase the source contact region and thereby to improve the on-resistance characteristics (see the description, page 6, lines 1-4). The objective technical problem can therefore be regarded as to improve the on-resistance characteristics.

4.4 In document D2 it is recognized (see section IV.A.) that the reduction of the size of the SC-UMOS, in particular the cell pitch, leads to a decrease of the source contact width, and therefore to an increase of the on-resistance. It is also reported in D2 that for small cell pitches the TC-UMOS has lower on-resistance values than the SC-UMOS, because the source contacts are formed at the sidewalls of the trenches and their width is thus constant regardless of the cell pitch.

The skilled person, a semiconductor physicist, seeking to improve the on-resistance characteristics of the SC-UMOS would therefore be led to consider the TC-UMOS design, rather than attempt to achieve yet another design with improved on-resistance characteristics. Therefore the skilled person would find it obvious to provide the intermediate structure shown in Figure 2(d) with - instead of an aluminium-silicon deposition to arrive at the SC-UMOS - contact trenches with boron ions implanted at the bottom, a tungsten deposition to fill the contact trenches, and aluminium to make source

and gate electrodes (see manufacturing steps (e) and (f) and Figure 2), thus arriving at the TC-UMOS.

4.5 Document D1 relates to a MOSFET like document D2 (see the description of Figure 1 in document D1a) and would therefore be considered by the skilled person for solving the objective technical problem. However, in the board's view, document D1 does not disclose feature (i) (see point 3.1 above) and therefore cannot lead the skilled person to the claimed invention.

4.6 The remaining prior art documents on file do not contain any teaching, either, leading the skilled person to the subject-matter of claim 1, which is therefore not considered to be obvious.

For corresponding reasons, the subject-matter of method claim 6 is not considered to be obvious, either.

The subject-matter of claims 2 to 5 and 7 to 12 is not considered to be obvious, as these claims are dependent on claims 1 and 6, respectively.

Accordingly, the subject-matter of claims 1 to 12 involves an inventive step (Article 52(1) EPC and Article 56 EPC 1973).

5. Other requirements of the EPC and conclusion

In order to comply with the requirements of Article 84 EPC 1973, the description has been brought into conformity with the amended claims. Furthermore, the description has been supplemented with an indication of the relevant content of the prior art to comply with

the requirements Rule 27(1)(b) EPC 1973. These requirements of the EPC are therefore also satisfied.

In view of the above the appellant's request is allowable.

Order

For these reasons it is decided that:

1. The decision under appeal is set aside.

2. The case is remitted to the first instance with the order to grant a patent on the basis of the following documents:

Description:	1, 1a, 2, 3	as filed during the oral proceedings
	4-7	as originally filed
Claims:	1-12	as filed on 21 December 2007 with the grounds of appeal (as Main Request)
Drawings:	Figures 1, 2A-D, 3A-C (Sheets 1-5)	as originally filed.

The Registrar: The Chairman:

S. Sánchez Chiquero G. Eliasson