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Datasheet for the decision of 8 December 2011

Case Number: T 1965/07 - 3.4.03

Application Number: 02000810.8

Publication Number: 1235277

IPC: H01L 27/146

Language of the proceedings: EN

Title of invention:
CMOS image sensor with complete pixel reset without kTC noise generation

Applicant:
Intellectual Ventures II LLC

Headword:
-

Relevant legal provisions (EPC 1973):
EPC Art. 54, 56, 84

Keyword:
"Main request: not supported by the description"
"Auxiliary request: allowable"

Decisions cited:
-

Catchword:
-

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Case Number: T 1965/07 **-** 3.4.03

D E C I S I O N
of the Technical Board of Appeal 3.4.03
of 8 December 2011

Appellant: (Applicant)
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Decision under appeal:
Decision of the Examining Division of the European Patent Office posted 18 July 2007 refusing European patent application No. 02000810.8 pursuant to Article 97(1) EPC 1973.

Composition of the Board:

Chairman: G. Eliasson
Members: V. L. P. Frank
P. Mühlens

Summary of Facts and Submissions

I. This is an appeal from the refusal of application 02 000 810 for the reason that the subject-matter of claim 1 of the main request was not new (Article 54 EPC 1973) and that the subject-matter of claim 1 of the 1st and 2nd auxiliary requests did not involve an inventive step (Article 56 EPC 1973).

II. At the oral proceedings before the board the appellant applicant requested that the decision under appeal be set aside and that a patent be granted on the basis of either claims 1 to 15 of the main request or on the basis of claims 1 to 14 of the first auxiliary request, both filed at the oral proceedings.

III. Independent claim 1 of the main request reads:

"1. A CMOS Active Pixel Sensor comprising:
an array of CMOS sensor pixels on a substrate, wherein at least one pixel comprises a photosensing vertical punch through transistor, having a source near the surface of the substrate, incorporated into the array of CMOS sensor pixels."

Independent claim 1 of the first auxiliary request reads:

"1. A CMOS Active Pixel Sensor comprising:
an array of CMOS sensor pixels (300) on a substrate, wherein at least one pixel comprises a photosensing vertical punch through transistor (203), having a source (405) near the surface of

the substrate (416), and a junction gate substantially surrounding and connected to the source; and a further gate (401, 604) substantially surrounding the junction gate (404)."

IV. The following prior art documents are cited in this decision:

D1: US 5 936 270 A

D2: JP 08 250 697 A and the corresponding English abstract.

At the oral proceedings before the board the appellant applicant submitted the following prior art document:

D2a: US 5 712 497 A

V. The examining division found

- that the CMOS sensor of claim 1 of the main request lacked novelty over the sensor disclosed in the embodiment of Figure 9 of document D1; and

- that the sensor according to claim 1 of the 1st and 2nd auxiliary requests did not involve an inventive step, since it was an obvious combination of the embodiments of Figures 8 and 9 of document D1.

VI. The appellant applicant argued essentially as follows:

- Document D2a was the US patent application family member of Japanese patent application D2. It was filed as an English translation of the latter.

- Document D2/D2a disclosed a bulk drain MOS image sensor (BDMIS) which, although similar in physical structure, worked in a completely different way than a vertical punch through transistor. In the BDMIS of D2/D2a the channel between source and drain was created by holding the gate 24 at the potential V_A so that a punch through between source and drain did not occur. In fact, a punch through between source and drain was expressly prevented by potential barrier $\Delta\phi_B$ formed under the semiconductor region 23.

- The statement on page 4b of the description of the present application according to which, for achieving the objects of the invention, the source of the transistor was surrounded by and connected to a junction gate, which was in turn surrounded by a gate, should not be seen as stating that these features were essential for carrying out the invention and that other embodiments were impossible. Claim 1 as originally filed did not contain these features and thus set out the broadest limits within which the inventors considered it feasible to carry out the invention. Claim 1 of the main request should therefore be allowable.

Reasons for the Decision

1. The appeal is admissible.

2. *Main request*

2.1 Claim 1 of this request is directed to a sensor comprising an array of CMOS sensor pixels on a substrate, wherein at least one pixel comprises a photosensing vertical punch through (VPT) transistor, having a source near the surface of the substrate.

2.2 The application as originally filed states that (page 4, Summary of the invention):

"The present invention relates to Active Pixel CMOS Image Sensors (APS) employing pixels that can be readout repeatedly and do not generate kTC noise. Such sensors have an advantage in efficient signal processing and subtracting the pixel signal response nonuniformities, since the inherent pixel temporal noise is very low and can be neglected. This leads to a superior low light level sensitivity and higher overall image sensing performance.

Incorporating the Vertical Punch Through (VPT) transistor into the CMOS sensor pixels, surrounding the source of the transistor by a junction gate that is connected to it, the junction gate being further completely surrounded by an MOS gate, achieves these and other objects of the invention."

Also the application's first preferred embodiment discloses that the VPT transistor consists of a p^+ type

doped source region 405 that is surrounded and connected to a p^+ type doped first junction gate region 404. The transistor further contains n type doped buried channel region 415 that is overlapped by the first polysilicon layer 401, which forms the second MOS transistor gate (page 11, lines 5 to 13; Figure 2). In the application's second preferred embodiment the field plate region 401 has been replaced by the polysilicon gate 604. The first junction gate region 404 remains however the same as in the previous embodiment (paragraph bridging pages 12 and 13; Figure 6). In the discussion on the working principles of the photosensing VPT transistor the bias of the first junction gate 404 plays a crucial role. It goes without saying that the shape and location of the gate 404 is also essential for the described working mechanism (paragraph bridging pages 11 and 12; Figure 5).

The photosensing VPT transistor has thus been consistently described in the application as comprising a junction gate surrounding and connected to the transistor's source, and a further gate surrounding the junction gate. Stating that the sensor pixel comprises merely a photosensing VPT transistor having a source near the surface of the substrate, as done in claim 1 of the main request, is in the board's view not supported by the description.

2.3 The appellant applicant argued that original claim 1 did not contain these features. In the original application the claims were headed "Summary of the invention" and the last paragraph on page 15 stated that: ***"It should be noted that objects and advantages of the invention may be obtained by means of compatible***

combination(s) particularly pointed out in the items of the following summary of the invention".

The board however is not persuaded that merely reiterating the wording of the claims under the heading "summary of the invention" at the end of the description would fulfil the requirement that the subject-matter of the claims be supported by the description. This would empty this requirement from any substantive content. In the board's view the area covered by the claims has to be proportionate to the invention's contribution to the state of the art. The present application has disclosed a single way of carrying out the invention and it is not apparent to the board that a skilled person could implement the invention by using a VPT transistor without a junction gate surrounding and connected to the transistor's source, and a further gate surrounding the junction gate.

2.4 The board finds, for these reasons, that claim 1 of the main request does not comply with Article 84 EPC 1973.

3. *1st Auxiliary request*

3.1 Claim 1 according to this request includes the further features defining the junction gate which were missing from claim 1 of the main request. It is therefore supported by the description.

3.2 The examining division objected that document D1 (Figure 9) disclosed:

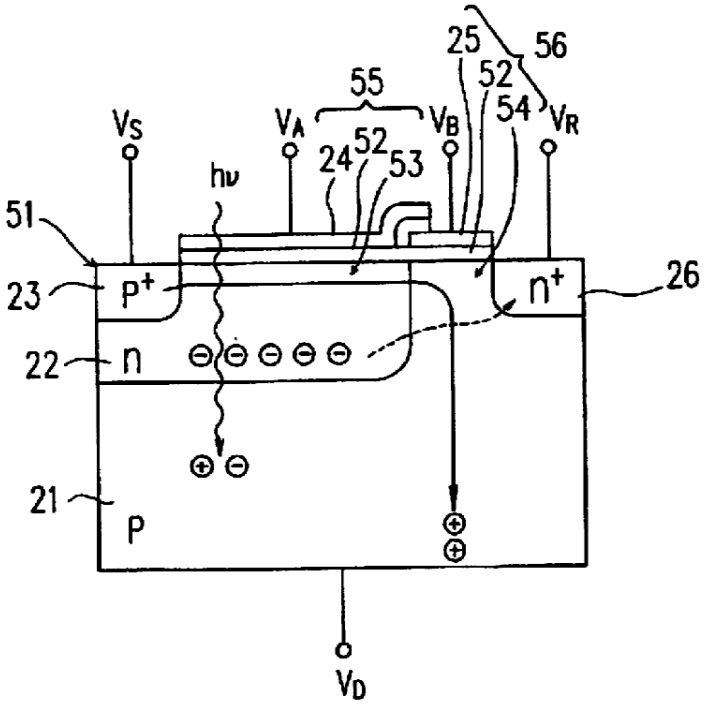
"A CMOS active pixel sensor having pixels with complete charge removal during pixel reset comprising an array of CMOS sensor pixels on a substrate (100) and a vertical punch through transistor (P^+ area connected to V_S, 104, n well and P_{sub} connected to V_D) having a source (P^+ area connected to V_S) incorporated into the array of CMOS sensor pixels, wherein the source is located substantially near the surface of the substrate of the sensor array and punches through a first junction gate region (104)." (reasons, B.1.1).

The objection of lack of novelty raised by the examining division thus boils down to the question of whether the device shown in Figure 9 of D1 is a vertical punch through transistor, something disputed by the appellant applicant.

3.3 When discussing this device D1 refers to *"the imaging device of a BDMIS (bulk drain MOS image sensor) type proposed in Japanese Laid-Open Patent Publication No. 8-250697"*, ie document D2 (D1, Example 4, column 11, line 60 to column 12, line 29; Figure 9). If the device of D2/D2a is not a vertical punch through transistor then neither is the device of D1 one.

In the following document D2a will be used as an English translation of D2 and all references will be made to this document.

3.4 Document D2a discloses an amplifying type photoelectric converting device. An n-type well 22 is formed inside a p-type semiconductor substrate 21 and a p^+-type semiconductor region 23 is provided in the well portion 22 in contact with the main surface 51. A first gate electrode 24 is formed on a region of the well 22 excluding the region 23 via an insulating film 52. A second gate electrode 25 is formed adjacent to the



first gate electrode. The first and second gate electrodes define respectively a first and second gate region 55 and 56. A voltage V_A is applied to the first electrode 24 so that a p channel for holes is formed in the surface proximate portion 53 in the first gate region 55. A voltage V_B is applied to the second electrode 25, so that the region of the substrate located below this electrode forms a p-channel. Therefore, a channel is formed for allowing a current in the form of holes to flow between the substrate 21

(the drain, to which a voltage V_D is applied) and the region 23 (the source, to which a voltage V_S is applied). Accordingly, the current of holes flows as indicated by the solid line (column 12, lines 25 to 56; Figure 1).

3.5 The board therefore agrees with the appellant applicant that document D2/D2a does not disclose a vertical punch through transistor, but a device in which current flows in the channel formed in the surface proximate portions 53 and 54. The control of the channel allows to sense the source-drain current and to readout the accumulated charges (column 13, lines 14 to 20).

Moreover, as the appellant applicant pointed out, a potential barrier against holes is formed below the semiconductor region 23 by controlling V_B, preventing thus a punch through in the vertical direction (column 15, lines 26 to 30).

3.6 It remains to be considered whether document D1 suggests modifying the device of D2/D2a so that it functions as a VPT transistor.

Document D1, however, relates to the use of an electric field strength buffering region for lowering the electric field strength between the source and drain regions of the transistor. The ion concentration gradient is sharp at and around the interfaces between the drain and source regions and the photoelectric conversion portion of the well region. This causes, according to D1, pseudo signal charges to be generated by impact ions, increasing dark current in the photoelectric conversion portion. To reduce the dark current an electric field strength buffering region 26

having a lower n type doping surrounds the n^+ type source region in the embodiments depicted in Figures 1 to 8 while a p type region 104 surrounds the p^+ type source region shown in Figure 9 (Figures 1 to 9 and the corresponding description).

Document D1 in no way suggests therefore to employ the device of D2/D2a, ie the device shown in Figure 9, in a different way than that disclosed in D2/D2a.

3.7 Thus neither document D1 nor D2 discloses or suggests using a VPT transistor in a pixel of a CMOS sensor. According to the application such a pixel avoids thermal kTC noise as the charges are completely removed from the pixel during reset (page 8; Figure 2). This can be considered as the objective technical problem addressed by the invention. As already stated there is no suggestion in the prior arts documents on file to use the solution proposed in the present application, namely to use a VPT transistor as a pixel of the sensor.

3.8 Consequently, the board finds that the CMOS sensor of claim 1 of the 1^{st} auxiliary request is new and involves an inventive step (Article 54 and 56 EPC 1973).

Order

For these reasons it is decided that:

1. The decision under appeal is set aside.

2. The case is remitted to the department of first instance with the order to grant a patent in the following version:

Description:

pages 1 to 4, 4a, 4b ,15 filed with letter dated 15 September 2006,
pages 5 to 14 as originally filed.

Claims:

1 to 14 of the first auxiliary request filed at the oral proceedings.

Drawings:

figures 1 to 6 as originally filed.

Registrar Chair

S. Sánchez Chiquero G. Eliasson