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Case Number: T 1586/07 - 3.4.03

Application Number: 99123516.9

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Language of the proceedings: EN

Title of invention:
Process for fabricating semiconductor device improved in step coverage without sacrifice of reliability of lower aluminium line

Patentee:
Renesas Electronics Corporation

Opponent:
-

Headword:
-

Relevant legal provisions:
-

Relevant legal provisions (EPC 1973):
EPC Art. 54(1),(2)
EPC Art. 56

Keyword:
"Inventive step (no) - main and first auxiliary request"
"Novelty (no) - second auxiliary request"

Decisions cited:
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Catchword:
-

Case Number: T 1586/07 - 3.4.03

D E C I S I O N
of the Technical Board of Appeal 3.4.03
of 12 October 2010

Appellant: Renesas Electronics Corporation
1753, Shimonumabe
Nakahara-ku
Kawasaki-shi
Kanagawa (JP)

Representative: Glawe, Delfs, Moll
Patent- und Rechtsanwälte
Postfach 26 01 62
D-80058 München (DE)

Decision under appeal: **Decision of the Examining Division of the European Patent Office posted 20 March 2007 refusing European patent application No. 99123516.9 pursuant to Article 97(1) EPC 1973.**

Composition of the Board:

Chairman: G. Eliasson
Members: R. Q. Bekkering
P. Mühlens

Summary of Facts and Submissions

I. This is an appeal against the refusal of application 99 123 516 for lack of inventive step, Article 56 EPC 1973, over document

D1: US 5 789 315 A.

II. At oral proceedings before the board, the appellant applicant requested that the decision under appeal be set aside and that a patent be granted on the basis of the main request or on the basis of one of the first or second auxiliary requests, all filed with letter of 10 September 2010.

III. Claim 1 of the main request reads as follows:

"A process for fabricating a semiconductor device, comprising the steps of:
a) forming a lower metal line (22) over a semiconductor substrate (20);
b) covering said lower metal line (22) with an inter-level insulating layer (23) under the condition that said semiconductor substrate (20) is heated to a first temperature at the maximum by depositing an insulating material by using a plasma-assisted chemical vapor deposition at said first temperature so as to form said inter-level insulating layer (23);
c) subsequently forming a via-hole (24) in said inter-level insulating layer (23);
d) carrying out an outgassing so as to remove contaminants from said inter-level insulating layer (23); wherein said outgassing is carried out under the condition that said semiconductor substrate (20) is

heated to a second temperature equal to or less than said first temperature; and
e) forming an upper metal line (30) penetrating into said via-hole (24) and extending on the exposed surface of said inter-level insulating layer (23) and formed of a conductive material selected from the group consisting of aluminum and aluminum alloys."

IV. Claim 1 of the first auxiliary request corresponds to claim 1 of the main request, in which, however, features b) and e) read as follows:

"*b) covering said lower metal line (22) with a single inter-level insulating layer (23) under the condition that said semiconductor substrate (20) is heated to a first temperature at the maximum by depositing an insulating material by using a plasma-assisted chemical vapor deposition at said first temperature so as to form said inter-level insulating layer (23)*";

"*e) forming an upper metal line (30) penetrating into said via-hole (24) and formed of a conductive material selected from the group consisting of aluminum and aluminum alloys.*"

V. Claim 1 of the second auxiliary request corresponds to claim 1 of the main request, in which, however, feature e) reads as follows:

"*e) forming an upper metal line (30) penetrating into said via-hole (24) and formed of a conductive material selected from the group consisting of aluminum and aluminum alloys.*"

VI. The appellant in substance provided the following arguments:

The subject-matter of claim 1 of all requests differed from document D1 in that it involved the formation of a single inter-level insulating layer whereas in D1 additional Spin-On-Glass (SOG) and other dielectric layers were formed on top. Furthermore, according to D1 the inter-level dielectric (ILD) had evolved into a complex structure. A deviation from this line of evolution of the ILD into a more and more complex structure and the finding that also a single layer might be sufficient for the ILD was not obvious to a skilled person, but required a completely new approach involving an inventive step. Moreover, the simplified process according to the invention required fewer steps and resulted in less thermal stress since the whole inter-level insulating layer was deposited at the same temperature. Therefore, the occurrence of hillocks and whiskers could be prevented, and the entire inter-level insulating layer was degassed by the outgassing step. Accordingly, the subject-matter of claim 1 of all requests was new and involved an inventive step.

Reasons for the Decision

1. The appeal is admissible.

2. *Main request*

2.1 *Novelty*

2.1.1 *Document D1*

Document D1 is concerned with a process for fabricating a semiconductor device and in particular with a process for forming the inter-level dielectric prior to via fill/metal deposition which substantially eliminates the problem of metal extrusions into the via regions. The process involves controlling the liner deposition temperature relative to temperature of the pre-metal deposition outgas step to control the thermal stress in the underlying metal line (column 3, lines 21 to 27).

In particular, document D1 discloses, using the terminology of claim 1, a process for fabricating a semiconductor device, comprising the steps of:

(a) forming a lower metal line (2) over a semiconductor substrate (cf figure 2A; column 2, lines 5 to 6; column 4, lines 10 to 13)

(b) covering said lower metal line (2) with an inter-level insulating layer (18) under the condition that said semiconductor substrate is heated to a first temperature at the maximum by depositing an insulating material by using a plasma-assisted chemical vapor deposition at said first temperature so as to form said inter-level insulating layer (cf figures 2A to 2C; column 2, lines 8 to 53; column 4, lines 14 to 31);

(c) subsequently forming a via-hole (6) in said inter-level insulating layer (cf figure 3; column 2, lines 54 to 60; column 4, lines 32 to 33);

(d) carrying out an outgassing so as to remove contaminants from said inter-level insulating layer, wherein said outgassing is carried out under the condition that said semiconductor

substrate is heated to a second temperature equal to or less than said first temperature (cf column 4, lines 34 to 40; column 5, lines 11 to 26); and

(e) forming an upper metal line (4) penetrating into said via-hole formed of a conductive material selected from the group consisting of aluminum and aluminum alloys (cf figure 1; column 1, lines 25 to 34; column 4, lines 4 to 6 and 34 to 40).

According to document D1, "*Following deposition of the conformal liner layer, the gap between metal lines may be filled with a dielectric 20 such as spin-on-glass (SOG), followed by an etch-back, resulting in a profile as shown in FIG. 2b. Additional layers of dielectric 22 may be deposited thereupon, to provide the desired thickness of dielectric separating the underlying metal from subsequently deposited metal layers, and to partially planarize the surface.*" (column 2, lines 45 to 52). Furthermore, "SOG layer 20 may be used to fill the gap between metal lines 2 as well as to aid in planarizing the ILD" (column 4, lines 18 to 20).

As apparent from figure 3 of D1, the upper metal line penetrating into the via-hole, would, in the via-hole, contact the inter-level insulating layer and thus arguably be "*extending on the exposed surface of said inter-level insulating layer*" as per feature e) of claim 1. For the purposes of this decision, however, the "*exposed surface*" is understood to be the upper/major surface of the inter-level insulating layer, as in substance argued by the appellant. Consequently, the inter-level insulating layer is a single layer formed by plasma-assisted chemical vapour deposition

(CVD), as opposed to document D1 in which an overlying SOG layer 20 and additional layers of dielectric 22 "*may*" be provided on top of the plasma enhanced chemical vapour deposition (PECVD) liner 18.

2.1.2 Accordingly, the subject-matter of claim 1 is new with respect to D1 (Article 54(1) and (2) EPC 1973).

2.2 *Inventive step*

2.2.1 The above distinguishing feature over D1 of forming a "*single*" inter-level insulating layer, rather than one with SOG and additional dielectric layers on top, provides a simpler manufacturing process.

Accordingly, the objective problem to be solved relative to D1 is to simplify the manufacturing process.

As indicated in D1, and well-known to the person skilled in the art, the SOG layer in D1 may be used to fill the gaps between metal lines as well as to aid in planarizing the inter-level dielectric layer (cf D1, column 4, lines 18 to 20). Depending on circumstances, eg where the spacing between the metal lines is relatively large and/or the step-height of the metal lines is small, the extra steps of applying SOG with corresponding etch-back for filling any gaps and planarizing the overall structure may be dispensable, as would readily occur to the person skilled in the art, thereby providing the process simplification sought. Similarly, it would readily occur to the skilled person to omit the not further specified additional layers of dielectric mentioned in D1, where these layer are

dispensable, further simplifying the manufacturing process.

In fact, as is apparent from the application as originally filed, it was known in the prior art to form the inter-level insulting layer by plasma enhanced CVD as a single layer of sufficient thickness to provide the required step coverage and overall dielectric separation (cf original application page 2, second and third paragraphs; figure 1B).

Accordingly, the person skilled in the art would revert to the as such well-known, simple single layer structure, without the exercise of inventive skills.

2.2.2 The appellant argued that according to D1 "*the ILD has evolved into a complex structure*" (column 2, lines 26 to 29). This appeared to be in contrast to the assumption that also a single layer might be sufficient for the ILD. In addition, the statement that the ILD was a complex structure also highlighted that it was common general knowledge of a skilled person that an ILD had a complex structure. Accordingly, a deviation from this line of evolution of the ILD into a more and more complex structure was not obvious to a skilled person, but required a completely new approach involving an inventive step. Simplifications often appeared to be obvious on the basis of hindsight, but, without the knowledge of the solution, were often more difficult to find than adding further features for overcoming problems. Moreover, the simplified process according to the invention required fewer steps and resulted in less thermal stress since the whole inter-level insulating layer was deposited at the same

temperature, so that the occurrence of hillocks and whiskers could be prevented and the entire inter-level insulating layer was degassed by the outgassing step.

2.2.3 Simplifications may indeed be difficult to find, if unexplored, but in the present case the simplification corresponds to the well-known prior art single-layer solution, commonly used as inter-level dielectric. The board cannot see any inventive merit in reverting to such an earlier, well-known solution. Furthermore, the ILD has evolved to a more complex structure, in particular one involving additional layers of SOG etc, for the very purpose of filling any gaps between metal lines and improving planarization. The skilled person would, therefore, be fully aware of the fact that the omission of the additional layers in the ILD would reduce complexity at the expense of accepting to dispense with the advantages that the complex ILD structure has. This cannot be held to be a new approach involving an inventive step as it merely reflects the skilled person's common sense to resort to complex solutions only when necessary.

As to the alleged benefits of less thermal stress in the layer and of degassing the entire layer, it is noted that they are associated with the provision of the inter-level dielectric as a single layer and thus are necessarily obtained when a single-layer solution is opted for.

2.2.4 Accordingly, the subject-matter of claim 1 according to the main request is obvious to a person skilled in the art and, thus, lacks an inventive step in the sense of Article 56 EPC 1973.

3. *First auxiliary request*

3.1 In claim 1 of the first auxiliary request, compared to that of the main request, in feature b) it is specified that the lower metal line is covered with a **single** inter-level insulating layer, whereas the feature that the upper metal line extends on the exposed surface of the inter-level insulating layer is removed from feature e).

3.2 Claim 1 as amended, like claim 1 of the main request, is understood to be only distinguished over D1 in that in D1 an overlying SOG layer 20 and additional layers of dielectric 22 "*may*" be provided on top of the PECVD liner 18.

This, however, cannot support inventive step, as discussed above for the main request.

Accordingly, the subject-matter of claim 1 according to the first auxiliary request is obvious to a person skilled in the art and thus lacks an inventive step in the sense of Article 56 EPC 1973.

4. *Second auxiliary request*

4.1 Claim 1 of the second auxiliary request neither defines a "*single*" inter-level insulating layer in feature b), as in the first auxiliary, nor does it define that the upper metal line extends on the exposed surface of the inter-level insulating layer, as in feature e) of claim 1 of the main request.

4.2 In the board's opinion, claim 1 as amended according to the second auxiliary request includes the possibility of having additional SOG and other dielectric layers on top of the plasma-assisted CVD inter-level insulating layer.

Accordingly, the above identified distinction between the subject-matter of claim 1 of both the main and the first auxiliary request over D1 is no longer provided in claim 1 of the second auxiliary request.

4.3 The appellant argued that claim 1 of the second auxiliary request excluded the provision of any additional inter-level dielectric layers.

It is, however, noted that the relevant wording of claim 1 corresponds in substance to that of claim 1 as originally filed, which, as detailed in dependent claim 6 as originally filed, did include the provision of additional SOG and other dielectric layers.

The mere addition in step c) of claim 1 of the second auxiliary request of the expression "*subsequently*", only specifies, in fact redundantly, that the step of forming the via hole in the inter-level insulting layer in the process sequence takes places after the layer is formed. It does not rule out any intervening process steps in which additional dielectric layers may be formed.

4.4 The subject-matter of claim 1 of the second auxiliary request, thus, is not new with respect to D1 (Article 54(1) and (2) EPC 1973).

Order

For these reasons it is decided that:

The appeal is dismissed.

Registrar	Chair
S. Sánchez Chiquero	G. Eliasson