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Datasheet for the decision of 21 September 2010

Case Number: T 1524/07 - 3.5.02

Application Number: 03809199.7

Publication Number: 1579575

IPC: H03L 1/00

Language of the proceedings: EN

Title of invention:
Improved phase locked loop

Applicant:
Nokia Corporation

Headword:
-

Relevant legal provisions:
EPC Art. 54, 123(2), 84

Relevant legal provisions (EPC 1973):
EPC R. 67

Keyword:
"Main and first and second auxiliary requests - novelty (no)"
"Third and fourth auxiliary requests - inadmissible extension (yes)"
"Fifth auxiliary request - not supported by description (yes)"
"Reimbursement of appeal fee - (no)"

Decisions cited:
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Catchword:
-

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Case Number: T 1524/07 - 3.5.02

D E C I S I O N
of the Technical Board of Appeal 3.5.02
of 21 September 2010

Appellant: Nokia Corporation
Keilalahdentie 4
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Representative: Higgin, Paul
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Decision under appeal: **Decision of the Examining Division of the European Patent Office posted 25 April 2007 refusing European patent application No. 03809199.7 pursuant to Article 97(1) EPC 1973.**

Composition of the Board:

Chairman: M. Ruggiu
Members: J.-M. Cannard
P. Mühlens

Summary of Facts and Submissions

I. The appellant contests the decision of the examining division of 25 April 2007 to refuse European patent application No. 03 809 199.7. The reasons for the refusal were, *inter alia*, that the subject-matter of claim 1 of the main request and the first to third auxiliary requests filed with a letter dated 26 January 2007 was not new (Article 54(1) EPC) and the first to fourth auxiliary requests filed by fax on 23 February 2007 were not admitted into the procedure.

II. With the statement of grounds of appeal filed with a letter dated 21 August 2007, the appellant filed sets of claims according to a main request and first to fifth auxiliary requests.

III. The prior art document:

D3: US2001/0036240 A1,

considered in the first instance, remains relevant to the present appeal.

IV. With a communication dated 17 May 2010 annexed to summons to oral proceedings, the Board observed, *inter alia*, that the subject-matter of independent claims 1 and 14 of the main request and the first and second auxiliary requests appeared to lack novelty having regard to document D3, claim 1 of the third and fourth auxiliary requests appeared to contravene Article 123(2) EPC, and the independent claims of the fifth auxiliary request did not seem to meet the requirements of Article 84 EPC.

V. With a letter dated 2 June 2010, the appellant announced that they would not attend or be represented at the scheduled oral proceedings.

VI. The appellant did not attend the oral proceedings before the Board which were held on 21 September 2010. It can be understood from the file as it stands that the appellant requests that the decision under appeal be set aside and that a patent be granted on the basis of the set of claims according to the main request, or of one of the sets of claims according to the first to fifth auxiliary requests, all filed with the statement of grounds of appeal in a letter dated 21 August 2007. Furthermore, the appellant requests reimbursement of the appeal fee.

VII. Claim 1 of the main request filed with the statement of grounds of appeal reads as follows:

"A frequency synthesiser, for providing an oscillating output signal (33) at an output frequency, comprising:

frequency compensation means arranged to maintain the output frequency; and

feedback means (110) arranged to introduce, in response to a change in the output frequency, a discrete coarse delay into a phase of an input signal (125) provided to the frequency compensation means, and an analogue fine delay into the phase of the input signal (125) wherein the coarse delay and the fine delay effect phase compensation of the input signal (125)."

VIII. Claim 1 of the first auxiliary request filed with the statement of grounds of appeal reads as follows:

"A frequency synthesiser, for providing an oscillating output signal (33) at an output frequency, comprising:

frequency compensation means arranged to maintain the output frequency; and

feedback means (110) arranged to introduce, in response to a programmed change in the output frequency, a discrete coarse delay into a phase of an input signal (125) provided to the frequency compensation means, and an analogue fine delay into the phase of the input signal (125) wherein the coarse delay and the fine delay effect phase compensation of the input signal (125)."

IX. Claim 1 of the second auxiliary request filed with the statement of grounds of appeal reads as follows:

"A phase-locked loop frequency synthesiser, for providing an oscillating output signal (33) at an output frequency, comprising:

frequency compensation means arranged to maintain the output frequency; and

feedback means (110) arranged to introduce, in response to a programmed change in the output frequency, a discrete coarse delay into a phase of an input signal (125) provided to the frequency compensation means, and an analogue fine delay into the phase of the input signal (125) wherein the coarse delay and the fine

delay effect phase compensation of the input signal (125)."

X. Claim 1 of the third auxiliary request filed with the statement of grounds of appeal reads as follows:

"A phase-locked loop frequency synthesiser, for providing an oscillating output signal (33) at an output frequency, comprising:

frequency compensation means arranged to maintain the output frequency; and

feedback means (110) arranged to introduce, in response to a programmed change in the output frequency, a one-off discrete coarse delay into a phase of an input signal (125) provided to the frequency compensation means, and an analogue fine delay into the phase of the input signal (125) wherein the coarse delay and the fine delay effect phase compensation of the input signal (125)."

XI. Claim 1 of the fourth auxiliary request filed with the statement of grounds of appeal reads as follows:

"A phase-locked loop frequency synthesiser, for providing an oscillating output signal (33) at an output frequency, comprising:

a counter (14, 24) for setting the output frequency using a counter parameter (M, N) to divide the frequency of a reference signal (21, 33);

a first control signal (35, 23) for changing the counter parameter (M, N);

frequency compensation means arranged to maintain the set output frequency; and

feedback means (110) arranged, in response to the output frequency, to provide a second control signal (121, 123) to introduce a one-off discrete coarse delay into a phase of an input signal (125) provided to the frequency compensation means and also to introduce an analogue fine delay into the phase of the input signal (125), wherein the coarse delay and the fine delay effect phase compensation of the input signal (125) following setting the output frequency."

XII. Claim 1 of the fifth auxiliary request filed with the statement of grounds of appeal reads as follows:

"A frequency synthesiser, for providing an oscillating output signal (33) at an output frequency, comprising:

frequency compensation means arranged to maintain the output frequency the frequency compensation means having an input signal (125); and

feedback means (110), the feedback means comprising means (14, 24) for introducing a discrete coarse delay into a phase of the first input signal (125) in response to a first control signal (121, 123) and means (106) for introducing a fine delay into the phase of the first input signal (125) in response to a second control signal (115), wherein

the feedback means (110) further comprises detection means (116) configured to detect when the second control signal (115) exceeds a predetermined threshold and in response to the detection that the second control signal (115) exceeds a predetermined threshold enable the first control signal (121, 123) to be provided and the second control signal (115) to be varied so that the value of the fine delay is adjusted to compensate for the introduction of the discrete coarse delay."

XIII. The appellant's arguments can be summarized as follows:

The subject-matter of claim 1 of the main request was novel because document D3 did not disclose:

- the introduction of a discrete coarse delay and an analogue fine delay into an input signal of frequency compensation means to effect phase compensation of this signal;

- these delays being provided in response to a change in the output frequency.

The delay introduced by the phase delay device 10 in D3 was not analogue because it had a value which was an integer multiple of T_{delmin} and did not take one of a continuous range of values. The delay added by the phase delay device 10 was not added when the frequency divider 9 switched from N to N+1. Thus, D3 did not disclose both a discrete coarse delay and analogue fine delay which were added to effect phase compensation of a signal.

Although the value of K was settable, there was no disclosure in D3 of feedback means which introduce coarse and fine delays in response to a change in the output frequency.

There was no disclosure in D3 of an analogue fine delay because the deladjust signal 11 merely set the delay of the elements in the phase delay device 10 as T_{delmin} which had a value of $1/(f_{VCO\text{-}setpoint}*M)$, and was neither an analogue nor fine delay.

D3 did not disclose that the discrete coarse and analogue fine delays were introduced in response to a programmed change in the output frequency, as recited in claim 1 of the first and second auxiliary requests. D3 was in fact primarily concerned with maintaining a particular output frequency and did not refer to a programmed change of the output frequency. The subject-matter of claim 1 of these requests was novel.

The independent claims of the third and fourth auxiliary requests were limited to the feature that the discrete coarse delay is a "one-off" delay. This feature did not introduce subject-matter which extended beyond the content of the application as original filed because the application and more specifically the passage at page 8, lines 8 to 10 did not indicate that the discrete coarse delay was set several times.

The fifth auxiliary request limited the claims to include the features that the frequency synthesiser comprises detecting means for detecting when the control signal provided to the fine delay means exceeds a predetermined threshold and for providing the

discrete coarse delay and an adjustment of the fine delay in response to this detection. Support for these features could be found on page 7, second and third paragraphs, of the filed application.

A substantial procedural violation which occurred during the examination proceedings justified the reimbursement of the appeal fees.

Reasons for the Decision

1. The appeal is admissible.

Main request

2. Document D3 discloses a fractional-N-based phase-locked loop (PLL) frequency synthesiser, thus a frequency synthesiser providing an oscillating output signal at an output frequency f_{vco} (Abstract; sections [0002] and [0009]; figure 2). The frequency synthesiser disclosed in D3 comprises all the features recited in claim 1 of the main request.

2.1 The phase-frequency detector 3, the control means comprising the charge pump 6 and the filter 7 and the negative feedback loop (frequency divider 9) can be seen as frequency compensation means arranged to maintain the output frequency f_{VCO}, within the meaning that these terms have in claim 1 (see for instance dependent claim 2 of the main request).

2.2 The PLL phase delay device 10, the phase accumulator 17 and the auxiliary PLL circuit 22, 23, 28, 29, 30 form

feedback means (see figures 2 to 4; sections [0047] to [0061]).

2.2.1 The phase delay device 10 comprises a variable number of elementary delay devices 16 controlled by a signal (DelSel 12), the delay of each elementary delay device being controlled by a further signal (DelAdjust 11), and thus provides an input signal 13 to the frequency compensation means. Since in response to the input signal 13 the content of the phase accumulator 17 is increased by the settable fraction K of the reference frequency f_{Ref} and sets the number of the elementary delay devices 16 (DelSel 12), the phase delay device 10 and the phase accumulator 17 can be seen as feedback means which introduce a discrete coarse delay into the input signal 13 when K is changed (sections [0051] and [0053]).

2.2.2 The auxiliary PLL circuit 22, 23, 28, 29, 30 produces an analogue signal, i.e. a continuously variable signal, (DelAdjust 11) in response to a change in the output frequency f_{VCO} and thus forms feedback means which introduce an analogue fine delay ($T_{delmin} = T_{VCO\text{-}setpoint}/M$) into the input signal 13 of the frequency compensation means (sections [0051], [0057] and [0059]).

2.3 D3 explains, in sections [0028] and [0053], that the parameter K is "adjustable" or "settable" and thus that its value can be changed. Modifying the value of the parameter K causes a change in the output frequency f_{VCO} (section [0009]). Thus, the phase delay device 10, the phase accumulator 17 and the auxiliary PLL circuit 22, 23, 28, 29, 30 are feedback means which introduce into an input signal provided to the frequency compensation

means, in response to a change in the output frequency f_{VCO}, discrete coarse and analogue fine delays which effect a phase compensation of the input signal 13 to the frequency compensation means. Accordingly, all the features of claim 1 are disclosed in D3 and the subject-matter of claim 1 of the main request lacks novelty (Article 54 EPC).

First and second auxiliary requests

3. Claim 1 of the first auxiliary request differs from claim 1 of the main request in that the change in the output frequency is a programmed change. Claim 1 of the second auxiliary request differs from claim 1 of the first auxiliary request in that it relates to a phase-locked loop frequency synthesiser. As appears from the foregoing, D3 discloses a phase-locked loop frequency synthesiser for providing an oscillating output signal at an output frequency and the value of the parameter K in D3 can be adjusted or set, i.e. programmed, whereby a change in the value of K appears to result in a programmed change in the output frequency. Accordingly, all the features of claim 1 of the first and second auxiliary requests are disclosed in D3 and the subject-matter of these claims lacks novelty (Article 54 EPC).

Third and fourth auxiliary requests

4. Claim 1 of the third and fourth auxiliary requests has been amended to specify that the discrete coarse delay is a one-off discrete coarse delay. The application as originally filed does not include the term "one-off". Apparently this term should indicate that the discrete coarse delay is introduced only once or, in other words,

that the introduction of a discrete coarse delay is not repeated. However, the application as filed states (see the published application WO2004/059844, page 10, lines 10 to 13) that "if the second control signal rises significantly above the threshold or the maximum threshold, then even after gross delay compensation at one cycle, it may still exceed the threshold in the next cycle, in which case gross delay compensation also occurs in the next cycle". It appears therefore that the gross delay compensation, i.e. the introduction of a discrete coarse delay, can be repeated and thus is not a "one-off" event. Accordingly, claim 1 of the third and fourth auxiliary requests contravenes Article 123(2) EPC.

Fifth auxiliary request

5. Claim 1 of the fifth auxiliary request does not meet the requirements of Article 84 EPC because it is not supported by the description.

5.1 As explained in the communication of the Board, in both embodiments described in the application, the discrete and continuously variable time delays are both introduced into an input signal to a phase comparator 16 of a phase locked loop (PLL) 100, and the values of these delays are dependent upon the output signal of the phase comparator 16. Claim 1 does not include these features and thereby defines matter that is not supported by the description in the sense of Article 84 EPC, in particular because it does not include all the features which, from the description, appear to be essential to carry out the invention.

6. Since the application according to the main and the first to fifth auxiliary requests does not meet the requirements of the EPC, the appeal has to be dismissed.

Reimbursement of the appeal fee

7. According to Rule 67 EPC 1973, the reimbursement of appeal fees shall be ordered where the Board of Appeal deems an appeal to be allowable. In the present case, the Board judges that the appeal has to be dismissed and the request for reimbursement of appeal fees is refused.

Order

For these reasons it is decided that :

1. The appeal is dismissed.

2. The request for reimbursement of the appeal fee is refused.

The Registrar: The Chairman:

U. Bultmann M. Ruggiu