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Case Number: T 1268/07 - 3.5.02

Application Number: 03019668.7

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Title of invention:
PLL clock generator circuit and clock generation method

Applicant:
Fujitsu Semiconductor Limited

Headword:
-

Relevant legal provisions:
EPC Art. 54

Relevant legal provisions (EPC 1973):
-

Keyword:
"Main, first and second auxiliary requests - novelty (no)"

Decisions cited:
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Case Number: T 1268/07 - 3.5.02

D E C I S I O N
of the Technical Board of Appeal 3.5.02
of 5 October 2010

Appellant: Fujitsu Semiconductor Limited
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Decision under appeal: **Decision of the Examining Division of the European Patent Office posted 7 February 2007 refusing European patent application No. 03019668.7 pursuant to Article 97(1) EPC 1973.**

Composition of the Board:

Chairman: M. Ruggiu
Members: J.-M. Cannard
E. Lachacinski

Summary of Facts and Submissions

I. The appellant contests the decision of the examining division to refuse European patent application No. 03 019 668.7. The reason for the refusal was that the application did not meet the requirements of Article 52(1) EPC, *inter alia*, because the subject-matter of claim 1 of the main request and auxiliary requests I and II then on file was not new (Articles 54(1) and (2) EPC), and claim 1 of the auxiliary requests III, IV and V then on file lacked an inventive step (Article 56 EPC).

II. The prior art document:

D1: US-A-6 160 861,

considered in the first instance, remains relevant to the present appeal.

III. With a letter dated 3 September 2010, the applicant filed new sets of claims according to a main request and first and second auxiliary requests. Claim 1 of the main request reads as follows:

"A clock generator circuit comprising:

a phase comparator (10; 20; 49; 62; 76) receiving a standard clock signal and an input operating clock signal and generating an output signal;

a charge pump (11; 21; 50; 63; 77) connected to receive the output signal of the phase comparator (10; 20; 49; 62; 76) and to supply a resulting signal;

a voltage controlled oscillator (13; 23; 53, 57, 58; 66, 72, 73; 80) generating an output operating clock signal (CLK; CLK2) based on the signal supplied by the charge pump, the voltage controlled oscillator comprising:

a voltage current converter (14; 24; 53; 66; 80) converting a voltage signal based on the signal supplied by the charge pump into a current signal;

a current D/A converter (15; 25; 57; 72; 81) arranged to receive the said current signal from the voltage current converter and to fluctuate the said current signal based on a digital control signal (27; 56; 71; 84) to produce a fluctuated current signal, the current D/A converter having a plurality of current sources that include current mirror circuits; and

a current controlled oscillator (16; 26; 58; 73; 82) arranged to receive the said fluctuated current signal and to oscillate the output operating clock signal (CLK; CLK2) with a variable frequency which corresponds to the fluctuated current signal, whereby the peak of the oscillation frequency spectrum of the output operating clock signal is dispersed."

Claim 5 of the main request reads:

"The clock generator circuit of any of claims 1 to 4, wherein the current D/A converter includes a determining circuit (29 to 33; 85 to 89) to determine the range of change of frequency of the output

operating clock signal oscillated by the current controlled oscillator."

IV. Claim 1 according to the first auxiliary request reads as follows:

"A clock generator circuit comprising:

a phase comparator (10; 20; 49; 62; 76) receiving a standard clock signal and an input operating clock signal and generating an output signal;

a charge pump (11; 21; 50; 63; 77) connected to receive the output signal of the phase comparator (10; 20; 49; 62; 76) and to supply a resulting signal;

a voltage controlled oscillator (13; 23; 53, 57, 58; 66, 72, 73; 80) generating an output operating clock signal (CLK; CLK2) based on the signal supplied from the charge pump, the voltage controlled oscillator comprising:

a voltage current converter (14; 24; 53; 66; 80) converting a voltage signal based on the signal supplied from the charge pump into a current signal that controls the oscillation frequency of a current controlled oscillator, wherein the oscillation frequency corresponds to the current signal;

a current D/A converter (15; 25; 57; 72; 81) arranged to receive the said current signal from the voltage current converter and to fluctuate the said current signal based on a digital control signal (27; 56; 71; 84) to produce a fluctuated current signal, the current

D/A converter having a plurality of current sources that include current mirror circuits; and

a current controlled oscillator (16; 26; 58; 73; 82) arranged to receive the said fluctuated current signal and to oscillate the output operating clock signal (CLK; CLK2) with a variable frequency which corresponds to the fluctuated current signal and which is centred on the frequency corresponding to the said current signal, whereby the peak of the oscillation frequency spectrum of the output operating clock signal is dispersed."

V. Claim 1 according to the second auxiliary request reads as follows:

"A clock generator circuit comprising:

a phase comparator (10; 20; 49; 62; 76) receiving a standard clock signal and an input operating clock signal and generating an output signal;

a charge pump (11; 21; 50; 63; 77) connected to receive the output signal of the phase comparator (10; 20; 49; 62; 76) and to supply a resulting signal;

a voltage controlled oscillator (13; 23; 53, 57, 58; 66, 72, 73; 80) generating an output operating clock signal (CLK; CLK2) based on the signal supplied by the charge pump, the voltage controlled oscillator comprising:

a voltage current converter (14; 24; 53; 66; 80) converting a voltage signal based on the signal

supplied by the charge pump into a current signal that controls the oscillation frequency of a current controlled oscillator, wherein the oscillation frequency corresponds to the current signal;

a current D/A converter (15; 25; 57; 72; 81) arranged to receive the said current signal from the voltage current converter and to fluctuate the said current signal within a range of +/- 20% based on a digital control signal (27; 56; 71; 84) to produce a fluctuated current signal, the current D/A converter having a plurality of current sources that include current mirror circuits; and

a current controlled oscillator (16; 26; 58; 73; 82) arranged to receive the said fluctuated current signal and to oscillate the output operating clock signal (CLK; CLK2) with a variable frequency which corresponds to the fluctuated current signal, which is centred on the frequency corresponding to the said current signal and which varies from its centre frequency within a range of +/- 20%, whereby the peak of the oscillation frequency spectrum of the output operating clock signal is dispersed."

VI. Oral proceedings were held on 5 October 2010 before the Board of appeal.

VII. The appellant requested that the decision under appeal be set aside and that a patent be granted on the basis of claims 1 to 9 of the main request (MR) filed with letter dated 3 September 2010, or subsidiarily on the basis of claims 1 to 9 of the first auxiliary request

(AR1) or the second auxiliary request (AR2) filed with the same letter.

VIII. The appellant's arguments can be summarized as follows:

According to claim 1 of the main request, the current D/A converter 15 received the current signal outputted by the voltage current converter 14 and fluctuated that current signal to produce a fluctuated current signal. In other words, the current D/A converter added a small perturbation to that current signal. Thus, the arrangement and function of the current D/A converter of claim 1 of the main request was not disclosed in document D1.

In D1, the IDAC 148 did not directly receive a current signal (CURRENT PROPORTIONAL CK) outputted by the voltage converter 119, but instead received a current signal IREF from a frequency to current converter 144.

In D1, the current from the integrator 119 was added to a signal 125B from a center frequency current generator 124. This combined current was provided to a reference ICO 140, a divider 142 and subsequently to the converter 144 which provided the current IREF to the IDAC. Hence, what was summed and fluctuated was the current IREF, not the current signal from a voltage current converter.

Further, according to claim 1 of the main request, the current controlled oscillator received the fluctuated signal outputted by the current D/A converter and produced a dispersed oscillation frequency accordingly.

In D1, the main ICO 126 received a control signal ICTL which combined the currents outputted from the center frequency current generator 124, the resistor 121, the feed forward compensation module 117 and the current IMOD from the IDAC. Thus, the frequency of the main ICO 126 did not correspond to the fluctuated current signal IMOD, but rather to a more complex current signal ICTL.

The subject-matter of claim 1 of the main request thus was new.

In claim 1 of the first auxiliary request, it was further stated that the clock signal "is centred on the frequency corresponding to the said current signal".

In D1, the clock frequency was controlled by the current ICTL which comprised in combination the current from a center frequency current generator 124, the current from the voltage current converter 119 through the resistor 121 and the fluctuated current IMOD. "Corresponding" should be understood as meaning "directly corresponding", but not as designating values which were "proportional". The centre frequency of the main ICO 126 was controlled not only by the current signal from the voltage current generator 119, but it was essentially determined by the current provided by the center frequency current generator 124 and thus it did not correspond to "the said current signal" as recited in claim 1 of the first auxiliary request which was new.

The subject-matter of Claim 1 of the second auxiliary request which specified a variable frequency of the output clock signal which varied from its centre

frequency within a range of +/-20% was new for the same reasons as claim 1 of the main and first auxiliary requests.

Reasons for the Decision

1. The appeal is admissible.

Main request - Scope of claim 1

2. The current A/D converter described in the application as filed (figure 11; page 14, line 20 to page 15, line 30) comprises a front step portion including current sources (transistors 29 to 33) and current mirror circuits (35-1 to 35-n). The front step portion receives a current signal Iin from the voltage current converter, determines the range of change of frequency of the output operating signal and controls the current mirror circuits (35-1 to 35-n) to fluctuate the current signal Iin. It provides the output operated clock signal Iout by adding the current from the front step portion and the currents from the current mirror circuits.

3. The current D/A converter of the clock generator circuit of claim 1 of the main request is arranged to receive a current signal from a voltage current converter and has a plurality of current sources that include current mirror circuits to fluctuate said current voltage.

3.1 Claim 5 appended to claim 1 specifies that the current D/A converter includes a determining circuit to

determine the range of change of frequency of the output operating clock signal.

3.2 Accordingly, claims 1 and 5, taken in combination and understood in the light of the description, cover a current D/A converter which includes a determining circuit receiving a current signal from the voltage signal converter and a plurality of current sources which produces a fluctuated current signal Iout. The current signal Iout corresponds to the sum of the currents provided by the determining circuit and the current sources including current mirror circuits.

Claim 1 of the main request - Lack of novelty

4. Document D1 discloses a clock generator circuit (figure 1; column 2, lines 49 to 67; column 3, line 33 to column 4, line 7; column 5, lines 22 to 55) that comprises the following features:

a phase comparator 110 receiving a standard clock signal (EXTERNAL REFERENCE CK) and an input operating clock signal and generating an output signal (MODULATED SYSTEM CK);

a charge pump 114 connected to receive the output signal of the phase comparator 110 and to supply a current signal (through resistors 121 and 123);

a current controlled oscillator generating an output operating clock signal (MODULATED SYSTEM CK) which is based on the current signal supplied from the charge pump 114 and oscillates with a variable frequency,

whereby the peak of the oscillation frequency spectrum of the output operating clock signal is dispersed.

4.1 As charge pumps conventionally output voltage signals, the charge pump 114 necessarily includes a voltage current converter to provide a current signal at its output. Therefore, the clock generator circuit shown in figure 1 of D1 can be understood as comprising a voltage controlled oscillator receiving a resulting signal from a charge pump 114 and comprising a voltage current converter outputting a current signal (through the resistors 121 and 123).

4.2 Accordingly, D1 discloses a clock generator circuit that comprises a phase comparator, a charge pump and a voltage controlled oscillator which includes a voltage current converter and a current controlled oscillator oscillating at a variable frequency, as recited in claim 1 of the main request. These considerations are not contested by the appellant.

5. The scope of claim 1 of the main request has to be understood as covering the features of dependent claim 5 (see above, the foregoing paragraphs 2. to 3.2). Thus, the scope of claim 1 is so broad that the remaining features specified in the claim are disclosed in D1. More specifically, the clock generator circuit of D1 comprises:

– a current D/A converter (140 to 148) comprising a determining circuit (140 to 146) to determine the range of change of frequency of the output operating clock signal (MODULATED SYSTEM CK) oscillated by the current controlled oscillator

(main ICO 126) and a plurality of current sources that include current mirror circuits (figure 1, 148; figure 2, 212 to 220) to fluctuate the said current signal based on a digital control signal (DAC controller 132) and to produce a fluctuated current signal IMOD, which is thus a current D/A converter with the meaning that these terms have in claims 1 and 5 taken in combination. The determining circuit, and thus the current D/A converter are arranged to receive a current signal through a resistor 123;

– a current controlled oscillator (ICO 126) arranged to receive the said fluctuated current signal IMOD and to oscillate the output operating clock signal (MODULATED SYSTEM CK) with a variable frequency which corresponds to the fluctuated current signal, whereby the peak of the oscillation frequency spectrum of the output operating clock signal is dispersed (column 1, lines 51 to 60).

6. Accordingly, D1 discloses a clock generator circuit which comprises all the features of a clock generator circuit which falls within the scope of claims 1 and 5 of the main request taken in combination. The subject-matter of claim 1 of the main request lacks novelty (Article 54 EPC).

7. The current D/A converter of claim 1 understood in the light of figure 11 of the present application also sums the current signal from the voltage current converter through a front step portion (i.e. a determining circuit) with the current fluctuated by the current mirror circuits to produce a fluctuated signal provided

to the current controlled oscillator. Such an arrangement is disclosed in D1 in which the current signal is summed at the output of a resistor 121 with the fluctuated signal IMOD. For this reason also, a current D/A converter arranged to receive a current signal from the voltage current converter, to produce a fluctuated current signal and to oscillate the output signal of a current controlled oscillator with a variable frequency is known from D1.

Claim 1 of the first auxiliary request - Lack of novelty

8. Claim 1 of the first auxiliary request differs from claim 1 of the main request in that it additionally specifies a current signal from the voltage current converter "that controls the oscillation frequency of a current controlled oscillator, wherein the oscillation frequency corresponds to the current signal" and a variable frequency "which is centred on the frequency corresponding to the said current signal". These additional features are based on page 9, lines 7 to 16; page 10, lines 16 to 20; page 14, lines 3 to 10; page 15, lines 17 to 21; and figures 2 and 4 of the application as originally filed.

9. It appears from the originally filed application (page 15, lines 10 to 30 and figure 11) that the current Iout supplied from IDAC 25 to the input of ICO 26 is always proportional to the current signal Iin, but is not centred on Iin for all ranges of fluctuation comprised within the range of +/- 20%. The term "corresponding" in the features incorporated in claim 1 of the first auxiliary request should be understood as having a meaning so broad as to cover the structure and

function of the only example of current D/A converter (IDAC) which is disclosed in the application. This meaning should be consistent with the meaning that this term has in the other feature added to claim 1 according to which "the oscillation frequency corresponds to the current signal" and in the passage on page 14, lines 20 to 22 of the description as filed which specifies that ICO 26... "oscillates the clock with the frequency corresponding to the current input Ii". Accordingly, "corresponding" in claim 1 of the first auxiliary request has to be understood as having a meaning like "proportional".

10. In D1, during normal modulated frequency operation, the current ICTL supplied to the input of the ICO 126 is the sum of the fluctuated current IMOD, a current 125A received from the center frequency current generator 124 and the current signal received from a voltage current converter (i.e. the current through resistor 121). When IMOD has a current value of zero, the ICO 126 oscillates with a center frequency on which the variable frequency is centred. This center frequency is proportional to the sum of the current 125A and the current through the resistor 121 which itself is proportional to the center frequency of the SYSTEM CLOCK (D1, column 4, lines 10 to 16 and column 5, lines 11 to 29; figure 1). Therefore, the variable frequency of the main ICO in D1 is centred on a frequency proportional to the current through the resistor 121, namely the frequency corresponding to the current signal from the voltage current converter with the meaning that has to be given to "corresponding" in claim 1. Accordingly, the features incorporated in claim 1 of the first auxiliary request are known from

D1. The clock generator circuit disclosed in D1 thus comprises all the features recited in claim 1 of the first auxiliary request whose subject-matter is not new (Article 54 EPC).

Claim 1 of the second auxiliary request - Lack of novelty

11. Claim 1 of the second auxiliary request differs from claim 1 of the first auxiliary request in that it specifies that the current D/A converter is arranged to "fluctuate the said current signal within a range of +/- 20%" and a variable frequency "which varies from its centre frequency within a range of +/- 20%".

12. In the clock generator circuit of D1, it is possible "to modulate the system clock by a precise percentage, such as 4% of the center frequency" (see column 5, lines 35 to 38), or by a percentage of 2% or 6% (column 6, lines 3 to 5). Therefore, in D1, the variable frequency of the main ICO 126 varies from its centre within a range falling in the claimed range of +/- 20%. The clock generator circuit disclosed in D1 thus comprises all the features recited in claim 1 of the second auxiliary request whose subject-matter is not new (Article 54 EPC).

13. Since the application amended according to the main and first and second auxiliary requests on file does not meet the requirements of the EPC, the appeal has to be dismissed.

Order

For these reasons it is decided that:

The appeal is dismissed.

The Registrar: The Chairman:

U. Bultmann M. Ruggiu