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Datasheet for the decision
of 29 May 2009

Case Number:	T 1191/07 - 3.4.02
Application Number:	02102078.9
Publication Number:	1285879
IPC:	B81C 1/00
Language of the proceedings:	EN

Title of invention:
Method of aligning structures on opposite sides of a wafer

Applicant:
Dalsa Semiconductor Inc.

Opponent:
-

Headword:
-

Relevant legal provisions:
-

Relevant legal provisions (EPC 1973):
EPC Art. 56

Keyword:
"Main request: inventive step (yes)"

Decisions cited:
-

Catchword:
-

Case Number: T 1191/07 **-** 3.4.02

DECISION
of the Technical Board of Appeal 3.4.02
of 29 May 2009

Appellant:	Dalsa Semiconductor Inc. 18 Airport Boulevard Bromont, Quebec J2L 1S7 (CA)
Representative:	Harding, Richard Patrick Marks & Clerk LLP 4220 Nash Court Oxford Business Park South Oxford OX4 2RU (GB)
Decision under appeal:	**Decision of the Examining Division of the European Patent Office posted 15 January 2007 refusing European application No. 02102078.9 pursuant to Article 97(1) EPC.**

Composition of the Board:

Chairman: A. G. Klein
Members: M. Stock
C. Rennie-Smith

Summary of Facts and Submissions

I. The applicant and appellant has appealed against the decision of the examining division refusing European patent application number 02102078.9 (published as EP 1 285 879 A1). Reference was made in that decision to the following documents:

D1: TATIC-LUCIC S ET AL: "NOVEL EXTRA-ACCURATE METHOD FOR TWO-SIDED ALIGNMENT ON SILICON WAFERS", SENSORS AND ACTUATORS A, ELSEVIER SEQUOIA S.A., vol. A42, no. 1/3, 15 April 1994 (1994-04-15), pages 573-577, XP000449984, LAUSANNE, CH, ISSN: 0924-4247

D2: TATIC-LUCIC S ET AL: "Silicon cultured-neuron prosthetic devices for in vivo and in vitro studies", SENSORS AND ACTUATORS B, ELSEVIER SEQUOIA S.A., LAUSANNE, CH, vol. 43, no. 1-3, September 1997, pages 105-1 09, XPOO41 03409 ISSN: 0925-4005, XP-004103409

D3: US-A-4 737 033

D4: BAER W G; NAJAFI K; WISE K D; TOTH R 5: "A 32-element micromachined thermal imager with on-chip multiplexing" SENSORS AND ACTUATORS A, vol. 48, 1995, pages 47-54, XP-004303571, CH

The examining division reasoned in particular that the subject-matter of the claims according to a main and an auxiliary request did not involve an inventive step. Moreover, the amended wording used in the claims according to the auxiliary request was not found in the original application, and, since this wording was not clear, it extended beyond the content of the application as originally filed.

II. In its statement of grounds of appeal the appellant requested the Board to set aside the decision of the examining division and grant a patent on the basis of the main request or the auxiliary request already presented before the examining division.

The appellant's arguments can be summarised as follows:

The object of the invention was to achieve alignment on opposite sides of a wafer in the manufacture of MEMS (micro-electro-mechanical systems) devices, such as pressure sensors, accelerometers, etc. In many of these applications, the formation of a hermetic seal was extremely important. The alignment was achieved by forming an alignment structure on the front side of the silicon wafer, converting portions of the bulk of the wafer to silicon oxide (thus creating transparent islands within the wafer), and etching from the back side of the transparent islands to permit alignment on the back side of the wafer to be performed with the alignment structures on the front side of the wafer by viewing the alignment structures through the transparent islands.

While the applicants were not concerned specifically with neurological devices, they nevertheless agreed that document D1 could be regarded as the closest prior art in that it addressed a similar problem, namely how to ensure alignment on opposite sides of a silicon wafer in generally the same field of endeavour.

Document D1 described a method of achieving this result wherein a low stress silicon nitride layer was coated on the front surface of the membrane and patterned with alignment marks. In one embodiment etching channels were patterned on the front side of the wafer with the alignment marks and subsequently etched with EPD or TMAH. In another embodiment, relevant to the present application, windows were formed in the backside of the wafer through to the membrane so that the alignment marks become visible from the backside of the wafer, thereby permitting subsequent alignment through these windows.

The preamble of claim 1 in the main request was amended to recite the steps of forming an alignment structure on the front side of the wafer, performing an anisotropic etch from the rear side to form a window through which the alignment structure becomes visible. This preamble was consistent with the teachings of D1. The applicants’ process differed from D1, as identified in the characterizing clause of claim 1, by the fact that portions of the wafer were converted to form transparent islands of silicon dioxide embedded in the wafer, and that the etching on the back side of the wafer extended only to the transparent islands embedded in the wafer, whereupon the alignment structures at the location of the islands could be viewed through the transparent islands.

MEMS devices to which the present method of aligning was applied required both mechanical and vacuum integrity since they often included cantilevered moving parts. The present application achieved these objectives because, unlike D1, it required no window to be opened completely through the wafer to a deposited layer, which in the case of a vacuum device was likely to be a source of leaks. Also, by making holes completely through the wafer as in D1, mechanical integrity was reduced. Therefore, in relation to D1, the objective technical problem could then be defined as a method of aligning the front and back sides of a wafer for use in a MEMS device that eliminates the potential source of leakage introduced by a deposited layer, and that does not involve making holes completely through the bulk wafer.

This objective technical problem was solved in accordance with the teachings of the present application by converting portions of the bulk wafer itself to silicon dioxide at alignment locations, recognising that silicon dioxide, unlike silicon, is transparent, and etching through the wafer from the back side only as far as the transparent islands.

Like D1, D2 was concerned with neurological devices, which was not directly a field of interest to the applicants, but nevertheless did relate to silicon micro-machine structures. D2 was not specifically concerned with back side alignment of wafers; it merely mentioned in passing in section 2 that precise front-to-back alignment on both sides of a (20 μm) silicon membrane was necessary to integrate the grillwork and the electrode with the well without explaining how the back side alignment was carried out. Therefore, since it related to a similar field, back side alignment was performed in the manner taught by D1.
D2 taught nothing about the problem relating to opening of holes all the way through the wafer in the alignment

process. Mechanical integrity would deter a person skilled in the art from finding any useful teaching in D2 with regard to the objective technical problem outlined above. However, if reading further one saw that D2 disclosed the use of LOCOS to form islands within the wafer. LOCOS was not new per se. However, LOCOS employed in D2 had nothing to do with the alignment process. D2 taught the use of LOCOS to create an array of islands of silicon in a field of silicon dioxide. This was the precise opposite of what the present application taught. In the present application transparent islands of silicon dioxide were formed in the bulk silicon. In D2, the silicon islands were covered with gold patterned into electrodes. They served an entirely different purpose. Moreover, there was no teaching in D2 that the silicon dioxide portions between the islands were transparent or any indication that such property would be useful in the manufacture of the device. D2 taught forming LOCOS islands in silicon, see, as explained in the first full paragraph, col. 2, on page 106, that "The LOCOS step is included in order to give the neurowell a dimpled bottom". Clearly, this taught nothing about solving vacuum problems in alignment processes nor did it hint at the fact that advantageous use could be made out of the fact that silicon dioxide is transparent.

III. Claim 1 according to the main request reads as follows:

"1. A method of aligning structures on front and rear sides of a silicon wafer for a MEMS device, wherein an alignment structure (18’) is fanned on the front side of the wafer (10), an anisotropic etch is performed on the rear side of the wafer (10) to form a window opening through which the alignment structure (18’) is visible, and precise alignment is carried out on the alignment structure (18’), characterized in that part of the bulk of the wafer (10) is converted on the front side of the wafer to form at least one transparent island (16) of silicon dioxide at an alignment location, the transparent island (16) having an exposed front side and a rear side embedded in the wafer (10), the anisotropic etch substantially reaches the rear side of the transparent island (16), the alignment structure (18’) is provided on the exposed front side of the transparent island (16), and the precise alignment is carried out on the alignment structure (18’) through the transparent island (16)."

The remaining claims 2 to 17 are appended to claim 1.

Reasons for the Decision

1. The examining division did not raise any formal objections to the claims of the main request, e.g. as to clarity, support by the description and original disclosure. The Board has also no reason to question the compliance of these claims with the above requirements of the EPC.

2. The Board agrees also about the finding of the examining division that the subject-matter of claim 1 is new, but disagrees with the examining division that this subject-matter does not involve an inventive step.

2.1 There is no doubt that document D1 is the closest prior art from which the subject-matter of claim 1 differs according to the characterising part in that

(i) part of the bulk of the wafer is converted on the front side of the wafer to form at least one transparent island of silicon dioxide at an alignment location;

(ii) the transparent island has an exposed front side and a rear side embedded in the wafer, the anisotropic etch substantially reaches the rear side of the transparent island;

(iii) the transparent island has an exposed front side and a rear side embedded in the wafer, the anisotropic etch substantially reaches the rear side of the transparent island;

(iv) the precise alignment is carried out on the alignment structure through the transparent island.

2.2 It will be evident from the analysis in points 2.3 to 2.7 below, that the concept underlying the claimed method is rather different from what is disclosed in D1. Therefore the objective problem to be solved by the claimed method is rather related to providing an alternative method to the one disclosed in D1, than to improving specific details of the known method, as was alleged by the examining division.

The Board cannot in this respect approve of the examining division's arbitrary tearing up of the actual contribution of the claimed method into separate aspects which it then considered in complete isolation from each other, namely the selection of an alternative material for the transparent layer, its patterning so as to form an island and the embedding of its back layer into the wafer. Having so misrepresented the claimed invention, the examining division then went on to question whether the two latter aspects individually achieved any technical function whatsoever, which led it to the somewhat simplistic conclusion that these aspects merely expressed the result of the choice between obvious alternatives, namely between an island shape or another shape (point 3.8 of the reasons) and between "embedding the rear surface or not embedding it" (point 3.9 of the reasons). This analysis does not in the Board's view amount to a fair and objective acknowledgement of the essence of the claimed method.

2.3 The concept of the present application is based on the recognition that the conversion of silicon into silicon dioxide on the front side according to step (i) leads to transparent islands (see page 5, lines 19 to 23) for observing the alignment structure formed on the transparent islands for effecting the alignment according to feature (iv) and serves the further purpose of an etch stop, see feature (ii), during etching of the wafer from the back side according to step (iii).

2.4 In D1, see page 573, right-hand column, second paragraph, two examples involving double-sided alignment using a premarked diaphragm in two common cases are presented. The first is double-sided alignment across a thin diaphragm (20 µm thick) and the second is across the whole 500 µm thick 4 inch silicon wafer. In the following section in D1, titled "Front-to-back alignment across a thin membrane" it is indicated that during the process a composite layer of 0.5 µm LTO and 1.0 µm PECVD Si_xN_y covering the front side is first patterned with the alignment marks, see Figures 1 and 2. Then by etching from the front side and the back side of the wafer the font side alignment mark is freed into a diaphragm with a small cavity underneath it. A heavily boron doped silicon layer used as an etch stop for etching from the back side is overetched from the small cavity side and thus provides an opening through which the front-side alignment mark becomes visible from the back side.

2.5 It is evident that the concept expressed by steps (i) to (iv) is quite different from this first example in D1. Even if the upper most layer of the three layer membrane shown in Figure 2 of D1 were made of pure silicon dioxide, the Board can see no obvious reasons which would have prompted the skilled person to form islands, to deposit the alignment marks on these islands and to use the islands as etch stops during etching of the windows from the back side.

2.6 According to the second example described in D1, see section titled "Front-to-back alignment across a whole wafer", page 547 in connection with Figure 5, the wafer is first coated with a 0.5 µm silicon nitride layer which is patterned with alignment marks. The alignment marks are freed by etching either through channels formed simultaneously with the alignment marks (see Figure 5(a)) or by opening etching windows on the back side of the wafer (see Figure 5(b)) and etching up to the front side.

2.7 If, for the reason of considering an alternate material, the skilled person decided to replace the silicon nitride layer described in accordance with the second example of D1 by a silicon oxide layer, further differences in terms of features (i) to (iv) of the claimed subject-matter would persist, which are in particular related to the formation of islands, on the exposed side of which the alignment marks are provided and the embedded side of which could be used as an etch stop. As far as islands are concerned, D2 discloses front-to-back alignment on both sides of a thin (20 µm) membrane. However, in D2 islands of silicon are in a field of oxide, whereas according to claimed subject-matter the islands consist of silicon dioxide, which is transparent, and are surrounded by silicon.

2.8 Documents D3 and D4 were cited by the examining division in order to show that the use of silicon oxide membranes formed in particular by thermal oxidation is known in connection with double-sided alignment. However, the structure of the devices obtained by the methods disclosed in D3 or D4 differ distinctly from what is obtained in accordance with the present invention.

2.9 In D3, see Figures 1 to 6 with the associated description in columns 2 and 3, the alignment mark formed by the openings 22 is covered by the thermal oxide layer formed on both surfaces of the substrate, whereas in accordance with the present invention the alignment mark is provided on the exposed surface of islands of silicon oxide.

2.10 D4, see Figures 1 and 2 with the relevant description, is related to a 32-element micromachined thermal imager based on thermopiles formed on a silicon oxide layer by a sequence of several method steps comprising deposition, patterning, doping and etching. The resulting device shows some structural similarity with the device of the present invention, in that in D4 there is also a patterned structure (metal of thermopile) formed on a silicon oxide layer which covers a window opened in the silicon substrate. However, the function is different due to the fact that in D4 infrared light is detected through the window opened in the substrate, whereas the window opening of the structure obtained by the method of the present invention serves the purpose of providing alignment of microstructures on opposite sides of a wafer by making an alignment mark visible.

2.11 Therefore the Board does not see how the skilled person starting from D1 would arrive at the subject-matter defined in claim 1 according to the main request in an obvious manner. Thus, this subject-matter involves an inventive step within the meaning of Article 56 EPC 1973.

3. The dependent claims are related to embodiments of the invention defined in claim 1. The description has been adapted to the amended claims. Therefore the Board is satisfied that a patent can be granted on the basis of the application documents as amended.

4. Since the appellant's main request is allowable, there was no need to discuss the auxiliary request or to appoint oral proceedings.

Order

For these reasons it is decided that:

1. The decision of the examining division is set aside.

2. The case is remitted to the first instance with the order to grant a patent in the following version:

<u>Description</u>:

Pages: 1 to 3, 6 to 12, 15 to 17 as originally filed.
Pages: 4 and 5 filed with letter dated 11 October 2006.
Pages: 13 and 14 filed with letter dated 27 May 2009.

<u>Claims</u>:

Nos.: 1 to 17 according to the main request filed with letter dated 11 October 2006.

<u>Drawings</u>:

Sheets: 1/9 to 9/9 filed with letter dated 10 October 2002.

The Registrar: The Chairman:

M. Kiehl A. G. Klein