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**Datasheet for the decision
of 9 April 2008**

Case Number: T 1153/07 - 3.5.02

Application Number: 00311746.2

Publication Number: 1220453

IPC: H03L 7/085

Language of the proceedings: EN

Title of invention:

PLL circuit with reduced settling time

Applicant:

Renesas Technology Corp., et al

Opponent:

-

Headword:

-

Relevant legal provisions:

EPC Art. 56

Relevant legal provisions (EPC 1973):

EPC R. 67

Keyword:

"Inventive step - after amendment (yes)"

"Reimbursement of the appeal fee - (no)"

Decisions cited:

-

Catchword:

See points 7 and 8 of the reasons



Case Number: T 1153/07 - 3.5.02

D E C I S I O N
of the Technical Board of Appeal 3.5.02
of 9 April 2008

Appellant: Renesas Technology Corp.
4-1, Marunochi 2-chome
Chiyoda-ku
Tokyo (JP)

Representative: Calderbank, Thomas Roger
Mewburn Ellis LLP
York House
23 Kingsway
London WC2B 6HP (GB)

Decision under appeal: Decision of the Examining Division of the
European Patent Office posted 26 February 2007
refusing European application No. 00311746.2
pursuant to Article 97(1) EPC.

Composition of the Board:

Chairman: M. Ruggiu
Members: J.-M. Cannard
P. Mühlens

Summary of Facts and Submissions

I. The appellant contests the decision of the examining division to refuse European patent application No. 00 311 746.2. The reason given for the refusal was that the subject-matter of claim 1 filed with letter of 20 December 2006 was considered to lack inventive step, Article 56 EPC.

II. The following documents of the state of the art, which have been cited in the first instance proceedings,:

D1: Yamawaki T. et al, "A 2.7-V GSM RF Transceiver IC", IEEE JOURNAL OF SOLID-STATE CIRCUITS, vol. 32, No 12, December 1997, pages 2089 to 2096,

D2: EP-A-0 856 946, and

D3: US-A-4 459 561,

remain relevant to the present decision.

III. Oral proceedings before the Board were held on 9 April 2008.

IV. The appellant requested that the decision under appeal be set aside and that a patent be granted in the following version:

Claims: 1 to 14 filed in the oral proceedings of 9 April 2008;

Description: pages 1 to 6, 11 to 22 as originally filed;
pages 6a, 7, 7a, 10 filed in the oral proceedings of
9 April 2008;

Drawings: sheets 1/15 to 15/15 as originally filed;

and that the appeal fee be reimbursed.

V. Independent claim 1 filed in the oral proceedings of
9 April 2008 reads as follows:

"A PLL circuit (402) comprising:

a phase comparator (100) with current mode output;
a low-pass filter (103);
a VCO (104); and
a logic circuit (711),

wherein the phase comparator output is fed to the low-
pass filter (103), and the low pass filter output signal
is inputted to the VCO (104) and the VCO output signal
corresponding to a PLL output signal is fed to the phase
comparator (100) to form a PLL feedback loop, and the
operation of the PLL feedback loop is controlled by the
logic circuit (711);

wherein:

in the case that a convergence frequency of the PLL
circuit (402) is lower than in (*sic*) the approximate
centre frequency of the PLL frequency range, the VCO
input voltage is first set to ground voltage, then the
VCO input voltage is increased by a constant current

source (101), and then the PLL circuit converges to the convergence frequency by the PLL feedback loop;

characterized in that:

in the case that a convergence frequency of the PLL circuit is higher than the approximate centre frequency of the PLL frequency range, the VCO input voltage is first set to a maximum voltage determined by the supply voltage, then the VCO input voltage is decreased by a further constant current source (200), and then the PLL circuit converges to the convergence frequency by the PLL feedback loop."

Claims 2 to 14 are dependent on claim 1.

VI. The appellant essentially argued as follows:

In the "tune mode" of document D3 the phase lock loop 110 was in an open loop state as appeared in particular from column 1, lines 55 to 61 and column 6, lines 60 to 62. Hence, D3 did not disclose an arrangement in which, where the convergence frequency of the PLL circuit was higher than the approximate centre frequency of the PLL frequency range, the PLL converges the convergence frequency by the PLL feedback loop.

Each of documents D1 and D3 offered a self-contained method of reaching the convergence voltage. They did not envisage a distinction between the case in which the input voltage is lower than the convergence voltage and the case in which the input voltage is higher than the convergence voltage.

As recorded in point 7 of the amended minutes of the oral proceedings, the examining division did not agree with the applicant's interpretation of the teaching of document D3 and took the view that the PLL loop of D3 remained in a closed state in the tune mode as well as in the lock mode. The applicant then asked the examining division to clarify which features of D3 they thought corresponded to the characterising part of the invention. However, the examining division refused the requested clarification, answering that the teaching of D3 was sufficiently clear and did not need to be explained further. Thus, it was evident that the examining division adopted an interpretation of document D3, in which the passage at column 1, lines 55 to 61, was given no weight. In oral proceedings, as in communications under Article 96(2) EPC (1973), applicants were entitled to understand the position of the examining division and their analysis of the prior art. In the absence of such understanding, it was impossible for the applicant to address the objections from the division. The refusal of the examining division to explain the technical nature of its objections was a procedural violation justifying the reimbursement of the appeal fee.

Reasons for the Decision

1. The appeal is admissible.

Current request - Admissibility of the amendments

2. The Board is satisfied that the claims and the description according to the current request meet the

requirement of Article 84 EPC and do not contravene Article 123(2) EPC.

- 2.1 This applies in particular to claim 1 which differs from claim 1 as originally filed in substance by referring to the logic circuit (711) which controls the operation of the PLL feedback loop, defining the connections between the components of the PLL circuit, and by the limitation that "in the case that a convergence frequency of the PLL circuit (402) is lower than the approximate centre frequency of the PLL frequency range, the VCO input voltage is first set to ground voltage, then the VCO input voltage is increased by a constant current source (101)" and "in the case that a convergence frequency of the PLL circuit is higher than the approximate centre frequency of the PLL frequency range, the VCO input voltage is first set to a maximum voltage determined by the supply voltage, then the VCO input voltage is decreased by a further constant current source (200)". These additional features are disclosed in figures 1, 3, 5 and 8 and in the description of the application as filed (see in particular column 7, lines 26 to 51 and column 8, lines 20 to 35 of the published application). Moreover, in view of figure 6 and the corresponding passage of the originally filed application (paragraph [0031] of the published application), the Board did not object to the replacement of "a setting frequency" by "the approximate centre frequency of the PLL frequency range". The Board has noticed an obvious clerical error indicated by (*sic*) in section V above. This obvious clerical error may be corrected by the examining division with the agreement of the applicant.

2.2 The original claims 3 and 4, 6 to 9, 11 to 14 and 16 to 18 have been renumbered, appended and adapted to amended claim 1.

2.3 The description has been adapted to the amended claims and a mention of the closest prior art known from document D2 has been included.

Current request - Novelty and inventive step

3. The subject-matter of current claim 1 is novel and involves an inventive step having regard to the cited prior art.

3.1 Document D2 which discloses a PLL circuit having all the components specified in the precharacterizing preamble of claim 1 can be taken as closest prior art (see figure 1 of D2). According to the embodiment described with reference to figure 1 of D2, the VCO input voltage is first set to ground voltage (switch 3), then increased by a constant current source (2), and then the PLL circuit converges to the convergence frequency by the feedback loop (column 4, line 38 to column 5, line 30). According to the circuit described with reference to figure 4 of D2, the VCO input voltage is first set to the supply voltage (power supply 8) by a switch (3), then decreased by a constant current source (2), and then the PLL circuit converges to the convergence frequency by the feedback loop (column 7, lines 6 to 50).

3.2 However, D2 does not disclose a PLL circuit which comprises both a constant current source to increase the VCO input voltage and a further constant current source

to decrease the VCO input voltage. Nor is the operation of the PLL feedback loop controlled by a logic circuit in accordance with a relationship between a convergence frequency of the PLL circuit and the approximate centre frequency of the PLL frequency range in such a way that the VCO input voltage is first set to ground voltage in the case that a convergence frequency of the PLL circuit is lower than the approximate centre frequency of the PLL frequency range, and first set to a maximum voltage determined by the supply voltage in the case that a convergence frequency of the PLL circuit is higher than the approximate centre frequency of the PLL frequency range. Therefore, the PLL circuit of claim 1 is novel having regard to the disclosure of D2.

- 3.3 Document D3 describes a circuit having a loop oscillator 10 and a PLL circuit 110 whose frequency is first tuned to approach the frequency of the loop oscillator 10 until the two oscillators lock. In the tune mode of D3, the VCO 112 of the PLL circuit 110 is swept from a high voltage +V by discharging a capacitor C1 by a constant current source 138 until the loop oscillator 10 and the VCO are locked in frequency. During tuning, the normal operation of the PLL loop (112, 144, 138, 154) is disabled because a low output is present on the D input of a flip flop 156, which maintains the phase comparator 144 in a given state and current sources 138 and 154 of the loop are not activated (see column 1, lines 55 to 68; column 4, line 20 to column 5, line 25; column 6, lines 56 to 68). In the lock mode of D3, the phase comparator and the current sources 138 and 154 are activated to enable the normal operation of the PLL loop which locks the VCO oscillator with respect to a reference frequency. The voltage Vc stored in the capacitor C1 adjusts itself

to obtain a stable cycle (column 7, lines 20 to 29; fig. 3) and the PLL circuit converges to a multiple of the frequency f_r of the reference oscillator which is near that at which the initial lock of the VCO with the loop oscillator occurred (column 6, lines 42 to 47; column 7, lines 26 to 30). Therefore, D3 does not mention any logic circuit for controlling the operation of the PLL feedback loop in accordance with a relationship between a convergence frequency and an approximate centre frequency of the PLL frequency range, as recited in claim 1. Moreover, the operation of the PLL feedback loop of D3, which is not activated in the tune mode, is not controlled so that the VCO input voltage is first set to a maximum voltage determined by the supply voltage, then decreased by a constant current voltage before the convergence of the PLL circuit to the convergence frequency, as recited in the characterizing part of claim 1. Nor can the PLL feedback loop of D3 be controlled so that the VCO input voltage is first set to ground voltage, then increased by a constant current voltage before the convergence of the PLL circuit to the convergence frequency.

- 3.4 None of the other prior art documents cited in the search report discloses a PLL circuit which comprises the features according to the characterising part of claim 1, namely wherein, in the case that a convergence frequency of the PLL circuit is higher than the approximate centre frequency of the PLL frequency range, the VCO input voltage is first set to a maximum voltage determined by the supply voltage, then the VCO input voltage is decreased by a further constant current source, and then the PLL circuit converges to the convergence frequency by the PLL feedback loop. This is

more specifically not the case for document D1, in which the VCO input voltage is first set to ground voltage, then the VCO input voltage is increased by a current source and then the PLL circuit converges. Hence, the subject-matter of claim 1 is novel (Article 54 EPC).

4. Starting from the PLL circuits of D2 and having regard to the effects provided by the PLL circuit set out in claim 1, the objective technical problem addressed by the invention can be seen as shortening the maximum convergence time of a conventional PLL circuit, which can be used in a mobile station of a GSM system as explained in the application in suit (paragraph [0013] of the published application).

5. There is no suggestion in any of the cited prior art to first set the VCO input voltage to a ground voltage in the case that a convergence frequency of the PLL circuit is lower than the approximate centre frequency of the PLL frequency range, and to first set the VCO input voltage to a maximum voltage determined by the supply voltage in the case that a convergence frequency of the PLL circuit is higher than said approximate centre frequency. Hence, in the judgment of the Board, the subject-matter of claim 1 involves an inventive step. More specifically:
 - 5.1 D2 discloses a PLL circuit for a portable terminal of a communication system. However, an approximate frequency centre of the PLL frequency range is not considered in D2. In the embodiments according to figures 1 and 4, which are independent from one another, the VCO input voltage is first set at an extreme point of the PLL range, either the ground voltage or the supply voltage,

unconditionally. D2 therefore does not suggest to a skilled person the idea of having in a same PLL circuit different initial settings of the VCO input voltage depending on a particular convergence frequency.

- 5.2 D3 relates to a vehicle detector installation which includes a first oscillator, the loop of which is laid in a roadway, and a PLL circuit which is first in a tune mode locked in frequency with the loop oscillator by sweeping the VCO input voltage from the supply voltage and then in the normal operation of the PLL circuit locked to a multiple of a reference frequency. There is thus no good reason for the skilled person wishing to minimise the convergence time of the PLL circuit according to figure 1 of D2 to consider the teaching of D3.
6. For the foregoing reasons, in the Board's judgment, the subject-matter of the claims of the current request is considered to be new and involve an inventive step within the meaning of Articles 54 and 56 EPC. The application as amended meets the requirements of the EPC.

Reimbursement of the appeal fee

7. Apparently, during the oral proceedings before the examining division, the division alleged that in document D3 "a working PLL is present in both modes, in the tune mode as well as in the lock mode" (point 7 of the amended minutes, first paragraph). In view of the passages of column 1 of D3, lines 55 to 61 and column 6, lines 59 to 66, the Board cannot share the examining division's interpretation of D3 (paragraph 3.3. *supra*). According to the established case law of the Boards of

appeal, an incorrect interpretation of the technical content of a prior art document constitutes an error of judgment and does not amount to a substantial procedural violation.

8. The question of whether "a working PLL is present in both modes, in the tune mode as well as in the lock mode" of D3, or not, was considered by the applicant in its letter of 20 December 2006 and during the oral proceedings before the opposition division. According to the point 7 of the amended minutes of 26 March 2007, the division pointed out that the PLL is not disconnected because "the switch SW4 only affects the connection of output 148 of the phase comparator 144 to the sink 138" They also asked the applicant if he had the intention of filing a request to overcome this objection before refusing the application (point 8 of the minutes). The applicant was thus given a reason for the objection raised and had an opportunity to reply to the examining division. The EPC does not require that more than one opportunity to present comments be given. Article 113(1) EPC thus was not contravened. In the circumstances, the refusal of the examining division to further explain the teaching of D3 does not appear to be a decisive factor for the refusal of the application. Therefore, the reimbursement of the appeal fee would in any case not be equitable. Therefore, the reimbursement of the appeal fee is refused (Rule 67 EPC 1973).

Order

For these reasons it is decided that :

1. The decision under appeal is set aside.
2. The case is remitted to the first instance with the order to grant a patent in the following version:

Claims: 1 to 14 filed in the oral proceedings of 9 April 2008;

Description: pages 1 to 6, 11 to 22 as originally filed;
pages 6a, 7, 7a, 10 filed in the oral proceedings of
9 April 2008;

Drawings: sheets 1/15 to 15/15 as originally filed.

3. The request for reimbursement of the appeal fee is refused.

The registrar:

The Chairman:

U. Bultmann

M. Ruggiu