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Datasheet for the decision of 2 February 2011

Case Number: T 1071/07 - 3.4.03

Application Number: 99905304.4

Publication Number: 1017100

IPC: H01L 27/06

Language of the proceedings: EN

Title of invention:
Three-dimensional device

Applicant:
Seiko Epson Corporation

Opponent:
-

Headword:
-

Relevant legal provisions:
-

Relevant legal provisions (EPC 1973):
EPC Art. 52(1), 54, 56

Keyword:
"Novelty (yes)"
"Inventive step (yes)"

Decisions cited:
-

Catchword:
-

Case Number: T 1071/07 - 3.4.03

D E C I S I O N
of the Technical Board of Appeal 3.4.03
of 2 February 2011

Appellant: Seiko Epson Corporation
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Decision under appeal: **Decision of the Examining Division of the European Patent Office posted 6 February 2007 refusing European application No. 99905304.4 pursuant to Article 97(1) EPC 1973.**

Composition of the Board:

Chairman: G. Eliasson
Members: V. L. P. Frank
P. Mühlens

Summary of Facts and Submissions

I. This is an appeal from the refusal of application 99 905 304 for the reason that the subject-matters of claims 1 and 4 of the main request and the subject-matter of claim 1 of the 1st and 2nd auxiliary requests did not involve an inventive step (Article 56 EPC 1973).

II. In response to a communication of the board the appellant applicant requested that the decision under appeal be set aside and that a patent be granted on the basis of the claim request submitted with letter dated 4 November 2010.

III. The claims of this request read as follows (the differences with respect to the version of the independent claims of the main request refused by the examining division was highlighted by the board):

"1. A three-dimensional device, comprising:
a substrate (21);
a first layer **(41)** that **is disposed on the substrate (21) and** includes a first memory cell array (71) **and a first connecting electrode (411), the first connecting electrode protruding from the first layer**;
a second layer **(43)** that includes a second memory cell array (72) **and a second and a third connecting electrode (431, 433), the second and third connecting electrodes protruding from the second layer** and ~~that is~~ **the second layer being** disposed on the first layer; and
a third layer **(42)** that includes a third memory cell array (73) **and a fourth connecting electrode**

(421), the fourth connecting electrode protruding from the third layer and ~~that is~~ **the third layer being** disposed on the second layer; **wherein:**
the first layer ~~including~~ **includes** a first input/output control circuit (741), a first row decoder (742) and a first column decoder (743); ~~and~~
the three-dimensional device ~~being~~ **is** configured such that the first input/output control circuit (741), the first row decoder (742) and the first column decoder (743) control the first memory cell array (71), the second memory cell array (72) and the third memory cell array (73), **and**
the first connecting electrode (411) and the second connecting electrode (431) are electrically connected to each other by way of an anisotropic conductive film (22), and the third connecting electrode (433) and the fourth connecting electrode (421) are electrically connected to each other by way of an anisotropic conductive film (23)."

"2. A method of manufacturing a device as claimed in any one of the preceding claims, the method comprising the steps of:
providing a first layer **(41)** that includes a first memory cell array (71) **and a first connecting electrode (411), the first connecting electrode protruding from the first layer** and ~~that is~~ **the first layer being** deposited on a substrate (21);
forming a first multi-layer structure including a second layer **(43)** that includes a second memory cell array (72) **and that includes a second connecting electrode (431) and a third connecting**

electrode (433), the second and third connecting electrodes both protruding from the second layer; and
disposing the second layer on the first layer by transferring the second layer from the **first** multi-layer structure to the first layer**, and electrically connecting the first and second connecting electrodes to each other by way of an anisotropic conducting film (22)**;
forming a second multi-layer structure including a third layer **(42)** that includes a third memory cell array (73) **and that includes a fourth connecting electrode (421), the fourth connecting electrode (421) protruding from the third layer**; and
disposing the ~~second~~ **third** layer **(42)** on the ~~third~~ **second** layer **(43)** by transferring the third layer from the second multi-layer structure to the second layer**, and electrically connecting the third and fourth connecting electrodes to each other by way of an anisotropic conductive film (23)**;
wherein the first layer further includes a first input/output control circuit (741), a first row decoder (742) and a first column decoder (743)**, that are** arranged to control the first memory cell array (71), the second memory cell array (72) and the third memory cell array (73)."

IV. The following prior art documents are cited in this decision:

D1: EP 0 986 104 A

D2: WO 95/09438 A

D3: US 5 089 862 A

V. The examining division found that the three-dimensional device of claim 1 and the manufacturing method of claim 4 of the main request as well as the device of claim 1 of the 1st and 2nd auxiliary requests did not involve an inventive step in view of document D2 and the general knowledge of the skilled person as exemplified by document D3.

However, due to the multiple amendments made to the claim request, the reasoning of the examining division is no longer relevant for the present decision.

VI. The appellant applicant argued essentially as follows:

- The claims were based on the arrangement shown in Figs. 16 and 23 of the application.

- D2 disclosed a plurality of layers, which were stacked one on top of the other and formed a three-dimensional device. In addition, ways of interconnecting the various layers were described. One way involved the use of via holes. In a second way, illustrated in Figs. 16A-16F, a hole in the layer was filled with an electrically and thermally conductive epoxy, coming thus into contact with the underlying metallization layer. A further metallization layer was deposited over the conductive epoxy. Neither of these techniques disclosed or suggested the use of an anisotropic conductive film to electrically connect mutually

facing connecting electrodes on the surfaces of the various layers, as now recited in the claims.

- Document D3 disclosed partially overlapping memory planes, but gave no clue as to how the circuitries of these planes interconnected.

- The claimed device had the following advantages: Firstly, it was easy to add another layer to the device, since the first layer contained the I/O control circuitry capable of driving all of the layers present. Hence it was possible to decide how many layers should be included during the manufacturing process itself. This, of course, involved providing the appropriate connecting electrodes on the surfaces of the various layers, so that signal routing could take place to each of the layers, including any additional layer decided on during the production process. Secondly, the interconnections between these electrodes were easily achieved by the use of anisotropic conductive films joining the various layers. With such films no unwanted signal paths occurred between electrodes on the same layer surface. Instead, signals flowed exclusively between electrodes on the surface of one layer and electrodes on the mutually facing surface of the next layer. Thus, any additional layer, which it was decided to introduce, could be easily incorporated using the connecting elements and associated anisotropic conductive layers. The use of such anisotropic layers avoided the need to form vias and deposit additional conductive tracks, as in D2 and D3. Thus, the use of anisotropic conductive layers avoided the need for photolithography

techniques, which were expensive, time-consuming and environmentally unfriendly. Consequently, the device of claim 1 could be formed faster, cheaper and with less wastage than the devices of the prior art.

Reasons for the Decision

1. The appeal is admissible.

2. *Novelty*

2.1 Document D1 is comprised in the state of the art under the provision of Article 54(3) EPC.

Although D1 discloses a three-dimensional device wherein the protruding electrodes of adjacent thin film layers are electrically connected to each other by an anisotropic conductive film ([0061] to [0063]), it does not disclose layers including memory cell arrays, input/output control circuits and row or column decoders.

2.2 Document D2 discloses a three-dimensional device comprising several layers of random access memory stacked on top of a multi-layer microprocessor. The address bus, data bus and control bus are routed up to the random access memory by the use of interlayer connectors (page 23, lines 29 to 34; page 24, lines 15 to 31; Figures 10 and 12). The connection between the layers are made either by via holes filled with metal (page 27, lines 20 to 31) or, alternatively, by a hole 430 etched through the epoxy layer 402 which attaches two adjacent layers 100, 200, exposing thus the

underlying metal pad 418, and depositing a further metal layer 432 which interconnects the exposed metal pads 418, 420 (page 19, lines 13 to 29; Figure 4B).

This document however does not disclose an anisotropic conductive film which electrically connects the protruding electrodes formed on the layers.

2.3 Document D3 discloses a possible architecture for a three-dimensional memory (column 34, line 60 to column 35, line 28; Figure 18). It does not disclose, however, how the interlayer connections are made.

2.4 The board finds for these reasons, that the device of claim 1 and the manufacturing method of claim 2 are new.

3. *Inventive step*

3.1 The sole document that discloses the use of anisotropic conductive films for connecting the electrodes of two adjacent thin film layers is document D1. As already mentioned (point 2.1), this document is comprised in the state of the art under the provision of Article 54(3) EPC. It is thus relevant for assessing novelty, but shall not be considered in deciding whether there has been an inventive step (Article 56 EPC 1973).

3.2 The board shares the view of the examining division that document D2 represents the closest state of the art.

The device of claim 1 differs from the three-dimensional device disclosed in this document in that

the memory cell array layers possess electrodes which protrude from these layers, that these electrodes are interconnected by anisotropic conductive films and that the control circuitry (encompassing by this expression the input/output control circuit and the row and column decoders) is formed on the first layer adjacent to the substrate.

3.3 The appellant has argued that in the claimed device it was easy to add a further memory layer, since the first layer contained the control circuitry capable of driving all the memory layers present. Hence it was possible to decide how many memory layers should be included even at such a late stage as during the manufacturing process itself. Furthermore, the interconnections between these electrodes were easily achieved by the use of anisotropic conductive films joining the various layers. The use of such anisotropic films avoided the need to form vias and to deposit additional conductive tracks, as in D2 or D3. Thus, the use of anisotropic conductive films avoided the need for photolithography techniques, which were expensive, time-consuming and environmentally unfriendly. The device of claim 1 could be formed faster, cheaper and with less wastage than the devices of the prior art.

3.4 The application as filed stated that it was an object of the invention to provide a high-performance three-dimensional device in which thin film device layers could be formed easily with versatility (original page 2, lines 13 to 15). Although this statement has been now deleted from the description, it can be used as a starting point for formulating the objective problem addressed by the invention as now claimed.

The objective problem can be formulated as to provide a three-dimensional device in which the thin film device layers can be easily electrically interconnected with improved design versatility.

3.5 This problem is addressed by the use of an anisotropic conductive film for interconnecting the protruding electrodes of adjacent thin film layers and by providing the control circuitry in the first layer adjacent to the substrate. As argued by the appellant, this allows to easily extend the number of memory cell array layers of the three-dimensional device. Neither D2 nor D3 suggest the use of anisotropic conductive films for interconnecting the device layers.

3.6 Consequently, the board finds that the three-dimensional device of claim 1 and the manufacturing method of claim 2 involve an inventive step within the meaning of Article 56 EPC 1973.

Order

For these reasons it is decided that:

1. The decision under appeal is set aside.

2. The case is remitted to the first instance with the order to grant a patent with the following documents:

   Claims:
   1 and 2 filed with letter dated 4 November 2010.

   Description:
   pages 1 and 7 to 77 as originally filed,
   page 2 filed with letter dated 4 November 2010,
   pages 3, 4 and 5 deleted,
   page 6 filed with letter dated 15 June 2005.

   Drawings:
   sheets 1/23 to 23/23 as originally filed.

Registrar / Chair

S. Sánchez Chiquero / G. Eliasson