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Datasheet for the decision of 11 March 2010

Case Number: T 0933/07 - 3.4.03

Application Number: 02026824.9

Publication Number: 1329946

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Language of the proceedings: EN

Title of invention:
Manufacturing method of semiconductor device including a laser crystallization step

Patentee:
SEMICONDUCTOR ENERGY LABORATORY CO., LTD

Opponent:
-

Headword:
-

Relevant legal provisions:
-

Relevant legal provisions (EPC 1973):
EPC Art. 56

Keyword:
"Inventive step (no)"

Decisions cited:
-

Catchword:
-

Case Number: T 0933/07 **-** 3.4.03

DECISION
of the Technical Board of Appeal 3.4.03
of 11 March 2010

Appellant:

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Representative:

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Decision under appeal:

Decision of the Examining Division of the European Patent Office posted 2 January 2007 refusing European patent application No. 02026824.9 pursuant to Article 97(1) EPC.

Composition of the Board:

Chairman: G. Eliasson
Members: R. Q. Bekkering
T. Bokor

Summary of Facts and Submissions

I. This is an appeal against the refusal of application 02 026 824 for lack of inventive step, Article 56 EPC 1973.

II. At oral proceedings before the board, the appellant applicant requested that the decision under appeal be set aside and that a patent be granted

- on the basis of claims 1 to 7, filed with letter dated 11 February 2010 (main request), or in the alternative,

- on the basis of claims 1 to 7 of the first auxiliary request filed with the grounds of appeal, or

- on the basis of claims 1 to 7 of the second auxiliary request filed with letter dated 11 February 2010.

III. Claim 1 of the main request reads as follows:

"*A manufacturing method of semiconductor device* [sic] *provided with a thin film transistor over a substrate (600) having an insulation surface, comprising:*
forming a non-monocrystal semiconductor layer (692) over said substrate (600); and
characterized by the steps of
patterning said non-monocrystal semiconductor layer (692) in accordance with a layout information of said thin film transistor to form a marker (544, 552) and an island-like semiconductor layer A (500, 529, 539),

wherein said island-like semiconductor layer A (500, 529, 539) is slightly larger than an area to become an active layer of said thin film transistor;
irradiating a laser beam selectively to said island-like semiconductor layer A (500, 529, 539) using said marker (544, 552) as a positional reference thereby irradiating only a part of the substrate surface; and patterning said island-like semiconductor layer A (500, 529, 539) by etching a periphery area thereof to form an island-like semiconductor layer B (501, 528, 538), which becomes said active layer area of said thin film transistor,
wherein said laser beam is a laser beam of pulse oscillation, and
the pulse width of said laser beam of pulse oscillation is 5Ons or more."

IV. Claim 1 of the first auxiliary request corresponds to claim 1 of the main request, in which however the second feature of the characterising portion of the claim reads as follows:

"applying a sequential super lateral growth method to a crystallization area (510, 511, 512) by irradiating a laser beam selectively to said island-like semiconductor layer A (500, 529, 539) using said marker (544, 552) as a positional reference thereby irradiating only a part of the substrate surface, wherein the relative position of the semiconductor layer with respect to the laser beam is shifted at each shot of the pulse and the crystallization proceed [sic] *in the direction of the shift;"*

V. Claim 1 of the second auxiliary request corresponds to claim 1 of the first auxiliary request with the following additional feature:

"*forming a channel region region* [sic] *(520, 530, 531, 532) in a region where an edge of the laser pulses exists*".

VI. Reference is made to the following prior art documents:

D4: PATENT ABSTRACTS OF JAPAN, vol. 1998, no. 04, 31 March 1998 & JP 09 320961 A, 12 December 1997 & US 6 657 154 B1, 2 December 2003

D7: US 4 409 724 A

D11: Robert S. Sposili and James S. Im, "Sequential lateral solidification of thin silicon films on SiO_2", Appl. Phys. Lett. 69(19), 4 November 1996, pages 2864 to 2866

VII. The appellant in substance provided the following arguments:

The specific selection of the pulse width as claimed guaranteed the presence of the required vertical temperature gradient in the semiconductor layer for the lateral growth of large crystal grains. It was the merit of the application to have established a suitable pulse width. This was described in particular with reference to figure 14 in the application. There was nothing in D11 to suggest the use of pulses with a duration other than the 30 ns disclosed. Moreover, documents D11 and D7 were silent as to the formation of markers and the use thereof for irradiating only a part of the substrate surface with the laser beam. The use of these markers had the advantage of increasing the efficiency of the recrystallisation process, not offered by the cited prior art. Accordingly, an inventive step had to be recognised for the subject-matter of claim 1 of the main request, or of at least any of the first or second auxiliary requests.

Reasons for the Decision

1. The appeal is admissible.

2. *Main request*

2.1 *Novelty*

2.1.1 *Document D7*

Document D7 is concerned with a method of fabricating a display with semiconductor integrated circuits combined therewith on the same substrate as a monolithic display structure. The substrate can be formed of a transparent material such as quartz or a glass on which polycrystalline semiconductor islands are disposed. Laser annealing of the polycrystalline semiconductor islands is relied upon to convert the polycrystalline semiconductor material of the islands to crystalline semiconductor material having an enhanced electron mobility characteristic sufficient to enable semiconductor devices, such as metal-oxide-semiconductor field effect transistors (MOSFETS), to be fabricated therein. In particular, the polysilicon islands are subjected to a laser annealing scan wherein the heat generated is at an intensity sufficient to cause recrystallisation of the polysilicon material in the islands to crystalline silicon having a substantially enlarged grain size and offering a much higher electron mobility characteristic than prior to the laser annealing treatment (column 2, line 66 to column 3, line 33).

2.1.2 In particular, document D7 discloses, using the terminology of claim 1, a method of manufacturing a semiconductor device provided with a thin film transistor over a substrate (10) of eg glass, ie having an insulation surface (cf column 6, line 55 to column 9, line 63; figures 1 to 8). The method comprises forming a polysilicon (ie non-monocrystal semiconductor layer) (11) over the substrate (10), patterning the non-monocrystal semiconductor layer (11) in accordance with a layout information of said thin film transistor to form an island-like semiconductor layer (14), wherein the island-like semiconductor layer (14) is slightly larger than an area to become an active layer of said thin film transistor (cf column 7, lines 51 to 64).

The method of D7 further comprises irradiating a laser beam selectively to the island-like semiconductor layer (14) and patterning the island-like semiconductor layer (14) by etching a periphery area thereof to form an island-like semiconductor layer which becomes the active layer area of said thin film transistor (cf column 7, line 65 to column 8, line 63).

2.1.3 Not disclosed in document D7 is patterning the non-monocrystal semiconductor layer in accordance with layout information of the thin film transistor to form a marker and irradiating the laser beam selectively to the island-like semiconductor layer using the marker as a positional reference thereby irradiating only a part of the substrate surface, as claimed.

Furthermore, in D7 an argon ion laser is used which is scanned with a line-to-line step size of the order of 7 µm (column 8, lines 5 to 10). Document D7, however, does not specify that the laser is pulsed and has a pulse width of 50 ns or more, as per claim 1.

2.1.4 Accordingly, the subject-matter of claim 1 is new with respect to D7 (Article 54(1) and (2) EPC 1973).

2.2 *Inventive step*

2.2.1 The above distinguishing feature over D7 concerning the formation and use of the marker makes it possible to irradiate only those parts of the substrate which actually require recrystallisation. As the scanning of the laser beam is a relatively slow process, this allows for a more expedient and efficient processing of the substrate.

Furthermore, as far as the above-mentioned distinguishing feature over D7 relating to the use of a pulsed laser with pulse widths of 50 ns or more is concerned, this contributes to improving the recrystallisation process so as to obtain larger crystal grains offering the high electron mobility sought.

Accordingly, the objective problem to be solved relative to D7 is on the one hand to increase the processing efficiency of the recrystallisation process and on the other hand to form larger crystal grains.

Although, as argued by the appellant, both the formation and use of the marker and the specified laser pulse width would ultimately improve the manufacturing method of D7, there is no functional interaction between the corresponding features which achieves a combined technical effect which is greater than the sum of the technical effects of the individual features, ie a synergistic effect. As no such synergistic effect exists, the features are merely aggregated and should be considered separately for their merits in terms of inventive step.

The board notes that both improving the process throughput of the recrystallisation process as well as improving the crystal grain size obtained with the recrystallisation are objectives, which would be obvious to a person skilled in the art working in the technical field of thin film transistor manufacturing at issue in the present case. The definition of the above problems to be solved as such, therefore, does not involve an inventive step.

2.2.2 *Document D11*

Document D11 discloses a process, named "*Sequential Lateral Solidification*", for recrystallising amorphous silicon using a laser beam so as to produce very large crystal grains, considered to be particularly suited for the manufacture of thin film transistors (page 2864, right-hand column, second paragraph; page 2865, left-hand column, second paragraph; page 2866, left-hand column, second paragraph). The process involves irradiating a pulsed laser beam on the sample while the sample is translated over a small distance between the pulses. The energy density of the laser pulse is such as to induce complete melting of the irradiated region. The distance of the micro-translations between the pulses is shorter than the single-pulse lateral solidification distance, so that lateral growth can be extended over a number of iterative steps thereby producing very large crystal grains. The process involves in particular exposing the sample to a pulsed XeCl excimer laser with a pulse duration of 30 ns and a pulse repetition rate of 1 Hz, while moving the stage between each pulse over a distance of 0.75 µm (page 2864, right-hand column, third paragraph; page 2865, left-hand column, second paragraph).

The document has in fact been cited in the application as originally filed (cf description pages 4 to 7).

2.2.3 The person skilled in the art, concerned with improving the crystal grain size obtained with the recrystallisation in D7 would consider applying the recrystallisation process of document D11, which provides the desired enlarged grains.

2.2.4 The appellant argued that it was the selection of the pulse width as claimed which guaranteed the presence of the required vertical temperature gradient for the lateral growth. It was the merit of the application to have established a suitable pulse width, as described in particular with reference to figure 14 in the application. There was nothing in D11 to suggest the use of pulses with a duration other than the 30 ns disclosed.

2.2.5 However, concerning the use of the specific 30 ns pulse excimer laser in D11, it would be readily apparent to the skilled person that other conventional laser equipment may be used, such as solid-state lasers widespread in industry, based on common considerations such as equipment availability and costs. Evidently, the use of other laser equipment having different characteristics such as the laser beam energy requires an adaptation of the process parameters including the pulse width.

As far as the selection of the specific pulse width of 50 ns or more as claimed is concerned, firstly it should be clear that the pulse width is merely one of the relevant process parameters and that in fact a number of other parameters ranging from the laser beam energy density to the layer thickness and material play essential roles in the recrystallisation process. Accordingly, any alleged advantage of the claimed method cannot be directly attributed to the selection of the pulse width only, as argued by the appellant.

Furthermore, according to D11 the irradiation energy density must be sufficiently high to induce complete melting of the exposed portion of the film (cf page 2866, left-hand column penultimate paragraph). This implies the presence of a vertical temperature gradient such that the semiconductor layer is molten throughout its thickness and solidification takes places laterally.

Accordingly, the skilled person faced with the task of selecting a suitable pulse width for a given laser would select the laser pulse width so as to obtain complete melting of the exposed portion of the film as prescribed by D11.

The claimed pulse width of 50 ns or more has been obtained by the applicant following the same considerations (cf description, paragraph bridging pages 15 and 16). In particular, as shown in figure 14 of the application, a pulse width of 50 ns or more is required for the underlying base film (and thus the bottom of the amorphous silicon layer) to reach a sufficiently high temperature, which is in fact near the melting temperature of amorphous silicon.

Thus, the skilled person, following the considerations above in relation to D11 and depending on the particular circumstances of the recrystallisation process, would arrive at pulse widths falling within the claimed range of pulse widths of 50 ns or more, without the exercise of inventive skills.

2.2.6 As far as the above problem of a more expedient and efficient recrystallisation process is concerned, it would readily occur to the skilled person that the recrystallisation process of D11, or indeed most scanned laser beam recrystallisation processes, are slow as they require scanning the substrate line-by-line with small translations in between. Furthermore, it would be readily apparent to the skilled person that there is no point in scanning the laser beam slowly over parts of the substrate not requiring any laser recrystallisation. Unlike in experimental setups like in D11 where this may not be of great concern, throughput is a major issue in a normal production environment for TFT displays such as those of document D7. It is therefore common practice to analyse each and every process and piece of equipment in order to reduce processing time and costs. Accordingly, it would be obvious to the person skilled in the art entrusted with the task of providing a more expedient and efficient recrystallisation process to only scan the laser beam over those areas actually requiring laser recrystallisation.

Furthermore, in order to be able to locate the relevant areas of the substrate requiring laser recrystallisation, it would readily occur to the skilled person to provide markers on the substrate and use the markers as a positional reference for directing the laser beam to the relevant areas of the substrate. Reference is made in this respect to document D4 disclosing a method of forming a semiconductor device with thin film transistors in which an amorphous silicon layer is provided on a substrate and recrystallised using a scanned laser beam. A marker is formed in the amorphous silicon film and subsequently used as a positional reference for detecting the region to be processed by laser recrystallisation (column 7, lines 34 to 48; column 7, line 63 to column 8, line 29; figures 7A to 7D and 8A to 8G).

Accordingly, it would be obvious to the skilled person to pattern the semiconductor layer in accordance with a layout information of the thin film transistors to form a marker and to irradiate the laser beam selectively to the island-like semiconductor layer using said marker as a positional reference thereby irradiating only a part of the substrate surface, as per claim 1.

2.2.7 Accordingly, the subject-matter of claim 1 according to the main request is obvious to a person skilled in the art and thus lacks an inventive step in the sense of Article 56 EPC 1973.

3. *First auxiliary request*

In claim 1 of the first auxiliary request the second feature of the characterising portion reads as follows:

"applying a sequential super lateral growth method to a crystallization area (510, 511, 512) by irradiating a laser beam selectively to said island-like semiconductor layer A (500, 529, 539) using said marker (544, 552) as a positional reference thereby irradiating only a part of the substrate surface, wherein the relative position of the semiconductor layer with respect to the laser beam is shifted at each shot of the pulse and the crystallization proceed in the direction of the shift".

Although the expression "*sequential super lateral growth method* " does not appear in the application as originally filed, for the purposes of this decision it is considered to be sufficiently clear that it refers to the "*sequential lateral solidification*" process of document D11, to which reference is made in the application as originally filed (cf page 4), and which is stated in D11 to be one of several processes collectively referred to as "*artificially controlled super lateral growth*" processes (cf D11, page 2865, right-hand column last paragraph). The further specification in the above feature that the relative position of the semiconductor layer with respect to the laser beam is shifted at each shot of the pulse and the crystallization proceeds in the direction of the shift in fact is nothing but a description of the very process of D11 as discussed above.

Accordingly, for the same reasons given above for the main request, the subject-matter of claim 1 according to the first auxiliary request lacks an inventive step in the sense of Article 56 EPC 1973.

4. *Second auxiliary request*

Claim 1 of the second auxiliary request corresponds to claim 1 of the first auxiliary request with the following additional feature:

"*forming a channel region region* [sic] *(520, 530, 531, 532) in a region where an edge of the laser pulses exists*".

In case the process of D11 is applied to D7, as argued above for the main and first auxiliary request, the laser beam is scanned over the channel region of the thin film transistor of D7 with micro-translations between pulses. Accordingly, in the course of the laser scan the "edge" of the laser beam "exists" in the channel region as per claim 1 of the second auxiliary request.

Accordingly, for the same reasons given above for the main and first auxiliary request, the subject-matter of claim 1 according to the second auxiliary request lacks an inventive step in the sense of Article 56 EPC 1973.

Order

For these reasons it is decided that:

The appeal is dismissed.

Registrar	Chair
S. Sánchez Chiquero	G. Eliasson