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Datasheet for the decision of 9 September 2010

Case Number: T 0827/07 - 3.5.02

Application Number: 96308327.4

Publication Number: 0806837

IPC: H03L 7/23

Language of the proceedings: EN

Title of invention:
Semiconductor integrated circuit operable as a phase-locked loop

Applicant:
Fujitsu Semiconductor Limited

Headword:
-

Relevant legal provisions:
EPC Art. 56
RPBA Art. 13(3)

Relevant legal provisions (EPC 1973):
-

Keyword:
"Inventive step - no (main request and first auxiliary request)"
"Admissibility of late-filed second auxiliary request - no"

Decisions cited:
-

Catchword:
-

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Case Number: T 0827/07 **-** 3.5.02

D E C I S I O N
of the Technical Board of Appeal 3.5.02
of 9 September 2010

Appellant: Fujitsu Semiconductor Limited
2-10-23 Shin-Yokohama
Kohoku-ku, Yokohama-shi
Kanagawa 222-0033 (JP)

Representative: Stebbing, Timothy Charles
Haseltine Lake LLP
Lincoln House, 5th Floor
300 High Holborn
London WC1V 7JH (GB)

Decision under appeal: **Decision of the Examining Division of the European Patent Office posted 27 November 2006 refusing European patent application No. 96308327.4 pursuant to Article 97(1) EPC 1973.**

Composition of the Board:

Chairman: M. Ruggiu
Members: M. Rognoni
E. Lachacinski

Summary of Facts and Submissions

I. The appellant (applicant) appealed against the decision of the examining division refusing European application No. 96 308 327.4.

II. In the contested decision, the examining division held, *inter alia*, that the subject-matter of claim 1 then on file did not involve an inventive step with respect to the following document:

D1: EP-A-0 493 607

III. With the statement of grounds of appeal dated 19 March 2007, the appellant filed a new set of claims 1 to 4.

IV. In a communication dated 27 April 2010 accompanying the summons to oral proceedings, the Board referred to the following new document:

D6: I. Novof *et al.*, "Fully Integrated CMOS Phase-Locked Loop with 15 to 240 MHz Locking Range and +/-50 ps Jitter," *IEEE J. Solid-State Circuits*, Vol. 30, No. 11, November 1995, pages 1259 - 1266.

V. With a letter dated 4 August 2010, the appellant filed a new set of claims 1 to 3 by way of auxiliary request.

VI. By fax dated 7 September 2010, the appellant filed new claims 1 to 3 by way of a second auxiliary request.

VII. On 9 September 2010, oral proceedings were held before the Board.

VIII. The appellant requested that the decision under appeal be set aside and that a patent be granted on the basis of claims 1 to 4 filed with the letter dated 19 March 2007 (main request), subsidiarily on the basis of claims 1 to 3 filed with the letter dated 4 August 2010 (first auxiliary request) or claims 1 to 3 filed with the letter dated 7 September 2010 (second auxiliary request).

Claim 1 according to the main request reads as follows:

"A semiconductor integrated circuit (10) generating a stabilized oscillation signal based on an input signal, the circuit comprising a plurality of unit circuits (20A, 20B) connected in series, each of said unit circuits having at least an oscillator (203), a divider (204), and a phase comparator (201) which form at least one part of a phase-locked loop; wherein:

a frequency of an oscillation output signal (203a-2) from said oscillator of a latter one (20B) of said unit circuits is higher than that of an oscillation output signal (203a-1) from said oscillator of a former one (20A) of said unit circuits, said oscillation output signal (203a-2) of said latter one of said unit circuits being said stabilized oscillation signal; and

each of said unit circuits further comprises a loop filter (202-1, 202-2); characterised in that :

each of said unit circuits (20A, 20B) is formed in the same LSI substrate for integrating a number of phase-locked loops with high density, but said loop filter (202-2) of the latter one (20B) of said unit

circuits has a time constant smaller than that of the loop filter (202-1) of the former one (20A) of said unit circuits, whereby the loop filter (202-2) of the latter one (20B) of said unit circuits generates an oscillation-frequency control signal (202a-2) having a larger control range of a control voltage than that (202a-1) generated from said loop filter (202-1) of the former one (20A) of said unit circuits;

the oscillator provided in the latter one (20B) of said unit circuits generates said oscillation output signal (203a-2) having a larger variation with respect to said control range of said control voltage than that of said oscillation output signal (203a-1) generated in the former one (20A) of said unit circuits;

the former one (20A) of the unit circuits further has differential output circuit (205) coupled with an output part of said oscillator (203-1), which converts said oscillation output signal (203a-1) of said oscillator (203-1) into a differential oscillation output signal (205a) to be transmitted to the latter one (20B) of said unit circuits; and

the latter one (20B) of the unit circuits further has a differential receive circuit (206) coupled with an input of said phase comparator (201-2), which receives said differential oscillation output signal (205a) transmitted from said differential output circuit (205) provided in the former one (20A) of said unit circuits, and converts said differential oscillation output signal (205a) into an input signal (11) of said phase comparator (201-2)".

Claim 1 according to the appellant's first auxiliary request differs from claim 1 of the main request in that it further comprises the following feature:

"and a dedicated power source (23A, 23B) is provided for each of said unit circuits (20A, 20B)."

Claim 1 according to the second auxiliary request differs from claim 1 of the first auxiliary request in that it comprises the underlined amendment:

"each of said unit circuits (20A, 20B) has substantially the same basic configuration and...".

IX. The appellant's arguments relevant to the present decision may be summarized as follows:

Document D1, which represented the closest prior art, showed a circuit for generating a stabilised oscillation which comprised two phase-locked loop (PLL) units connected in series. This document, however, did not provide any information concerning the time constant of the loop filters or the gain of the oscillator. Furthermore, as shown in Figure 5(a), there was a one-line connection between the two PLLs.

The subject-matter of claim 1 according to the main request differed from the circuit known from D1 in that it further comprised features relating to the time constants of the loop filters, the range of the control voltage generated by the loop filters, the variation of the oscillation output signal generated by the voltage controlled oscillators (VCO) and the differential architecture for connecting the two PLLs.

None of the cited documents suggested selecting the time constants as indicated in claim 1. However, even if it were assumed that a person skilled in the art would choose the time constants as claimed and that, as a consequence of the time constant selection, the range of the control voltage generated by the first loop filter was larger than the one generated by the second loop filter, this skilled person would not arrive at the claimed circuit because the prior art did not suggest increasing the variation of the oscillation output signal by selecting the second oscillator so that the ratio between the frequency range and the control signal range was greater in the second oscillator than in the first.

The remaining features of claim 1 were directed to increasing the stability of operation of the circuit of the invention and to making it more immune to noise by adopting a differential link between the two PLLs. There was no suggestion in any of the cited prior art documents of providing a differential output between two unit circuits of a semiconductor integrated circuit as now claimed. Document D6 related to a single PLL and did not teach to use a two-wire line to connect two PLLs in series. In fact, as specified in the present application, the differential output of the first oscillator required necessarily that this two-wire signal be converted into a single-ended signal to be fed to the comparator in the second PLL. There was no indication in the cited prior art as to how this could be done.

Claim 1 according to the first auxiliary request further specified that a dedicated power source was provided for each of the unit circuits of the claimed circuit. This feature further distinguished the circuit of the invention from the cited prior art.

The second auxiliary request was late filed but involved only a simple and immediately understandable amendment.

Reasons for the decision

1. The appeal is admissible.

Main request

2.1 Claim 1 according to the appellant's main request relates to a *"semiconductor integrated circuit (10) generating a stabilized oscillation signal based on an input signal"* and comprises the following features:

(a) a plurality of unit circuits connected in series,

(a1) each of said unit circuits having at least an oscillator, a divider, and a phase comparator which form at least one part of a phase-locked loop; wherein:

(a2) a frequency of an oscillation output signal from said oscillator of a latter one of said unit circuits is higher than that of an oscillation output signal from said oscillator of a former one of said unit circuits, said oscillation output

signal of said latter one of said unit circuits being said stabilized oscillation signal; and

(b) each of said unit circuits further comprises a loop filter;

(c) each of said unit circuits is formed in the same LSI substrate for integrating a number of phase-locked loops with high-density,

(d) said loop filter of the latter one of said unit circuits has a time constant smaller than that of the loop filter of the former one of said unit circuits, whereby

(e) the loop filter of the latter one of said unit circuits generates an oscillation-frequency control signal having a larger control range of a control voltage than that generated from said loop filter of the former one of said unit circuits;

(f) the oscillator provided in the latter one of said unit circuits generates said oscillation output signal having a larger variation with respect to said control range of said control voltage than that of said oscillation output signal generated in the former one of said unit circuits;

(g) the former one of the unit circuits further has differential output circuit coupled with an output part of said oscillator, which converts said oscillation output signal of said oscillator into a differential oscillation output signal to be

transmitted to the latter one of said unit circuits; and

(h) the latter one of the unit circuits further has a differential receive circuit coupled with an input of said phase comparator, which receives said differential oscillation output signal transmitted from said differential output circuit provided in the former one of said unit circuits, and converts said differential oscillation output signal into an input signal of said phase comparator.

2.2 Document D1 (see Figures 5(a), 5(b) and 5(c)) relates to a semiconductor integrated circuit 10 (see reference to "IC" in D1, page 8, lines 5 and 6) having the following features expressed in the language of claim 1:

– two unit circuits 11 and 12 connected in series (feature (a));

– each of said unit circuits has an oscillator 11b, 26, a divider 11c, 25 and a phase comparator 11d, 22 which form one part of a phase-locked loop (feature (a1));

– a frequency fp of an oscillator output signal from said oscillator of the second one of said circuits is higher than that of an oscillation output signal fp/n from said oscillator of the first one of said unit circuits, said oscillation output signal of said second one of said unit circuits being said stabilized oscillation signal (feature (a2));

– each of said unit circuits further comprises a loop filter 11e, 23, 24.

2.3.1 The subject-matter of claim 1 differs from the circuit shown in D1 in that it further comprises features (c) to (h).

2.3.2 Features (c) to (h) cover different aspects relating to the implementation of a frequency generator based on two cascaded PLLs which are familiar to the person skilled in the art. Such aspects of circuit design concern in particular circuit integration, the selection of the time constant of the loop filters, the control range and the frequency range of the VCO in a PLL and the reduction of its sensitivity with respect to substrate and power supply noise.

2.3.3 Starting from D1, the problem addressed in the present application can be seen in implementing the frequency generator according to D1 as an integrated circuit with a stable high-frequency oscillation output signal (cf. application as filed, page 4, lines 15 to 22).

2.4.1 Feature (c) specifies that each phase-locked loop (PLL) unit is formed in the same LSI substrate for integrating a number of phase-locked loops with high density.

2.4.2 Fully integrated PLL circuits are generally known in the art (see e.g. D6, Abstract) and a skilled person is well aware of the advantages in terms of cost and reliability that are offered by fully integrated circuits. It would thus be obvious to the skilled

person to integrate the two cascaded PPLs of the circuit of D1 into a common substrate.

2.5.1 Feature (d) relates to the selection of the time constant of the loop filter of the first and second PLL units.

2.5.2 As correctly observed by the examining division, it is normal practice in the art of PLLs to select the cut-off frequency of the low pass filter (loop filter) according to the reference frequency and, in particular, to make it equal to a fraction of such reference frequency. The application of this principle to the two cascaded PLLs of D1 implies that the cut-off frequency of the first loop filter is lower than the cut-off frequency of the second loop filter. It is also generally known that there is an inverse relationship between the cut-off frequency of a low pass filter and its time constant, so that a filter with a higher cut-off frequency has a smaller time constant than a filter with a lower cut-off frequency.

2.5.3 In other words, a person skilled in the art wishing to implement a circuit comprising two cascaded PLL units as known from D1 would necessarily select for the second PLL unit, which uses the output frequency of the first PLL unit as reference frequency, a loop filter with a smaller time constant than the loop filter of the first PLL unit. Feature (d) relates therefore to a parameter that the skilled person would necessarily select when implementing the circuit of D1.

2.6.1 Feature (e) is concerned with the "control signal" generated by the loop filter and specifies essentially

that the range of control voltage generated by the loop filter with the smaller time constant is larger than the range of control voltage generated by the loop filter with the larger time constant.

2.6.2 As specified in the description of the present application (application as filed, page 21, lines 14 to 32), this effect is achieved when the time constant of the second loop filter is smaller than the time constant of the first loop filter. Thus, as observed by the examining division, feature e) is a direct consequence of feature d).

2.7.1 As explained by the appellant, feature (f) implies that the oscillator of the second PLL has a gain larger than the gain of the first oscillator. Although the respective gains G_1 and G_2 of the oscillators of the first and second PLLs can in principle be selected so that $G_1 > G_2$, $G_1 = G_2$ or $G_1 < G_2$, the examining division has correctly noted that in practice only two options, *i.e.* $G_1 > G_2$ and G1 < G_2, are available to the skilled person, since it would be impossible to implement two oscillators with identical gains.

2.7.2 According to the description of the present application (application as filed, page 20, line 19 to page 21, line 22) the *"control performance"* of the oscillation output signal in a PLL is expressed as the ratio δf /f of the *"variable frequency range δf of the oscillation output signal"* to the oscillation frequency f. If the variable frequency range is supposed to be the same for both PLLs, *i.e.* $\delta f_1 = \delta f_2$, the ratio δf /f will depend on the output frequency f_1 and f2 and will decrease as the frequency f increases. Feature (e) provides a

solution to this problem by increasing the range of the control range δV_2 of the oscillation frequency control signal of the oscillator in the second PLL . However, it is evident that the effect of feature (e) would be reduced and possibly cancelled out, if G_2 were not selected to be larger than or at least equal to G_1. For this reason and because of the fact that only $G_2 > G_1$ is actually technically feasible, the skilled person would inevitably select the two PLL oscillators so as to satisfy the relationship specified in feature (f).

2.8.1 As pointed out by the appellant, features (g) and (h) restrict the claimed circuit to one in which a differential output is provided from the first PLL to the second PLL.

2.8.2 D6 (see Abstract) relates to a *"fully integrated phase-locked loop (PLL)"* implemented in CMOS technology. As specified on page 1259, left-hand column, bottom paragraph, a *"standard digital CMOS process is used to produce differential circuits that are designed to reduce their sensitivity to substrate and supply noise".*

2.8.3 The appellant has however stressed that none of the cited prior art documents suggested using differential architecture for a circuit comprising two cascaded PLL units. In fact, such an arrangement required a *"differential receive circuit"* (see feature (h)) to convert the differential oscillation output signal of the first PLL into an input signal for the comparator of the second PLL unit. As D6 did not show how to adapt the differential output of a PLL unit to a single-line input, it would not be obvious to the skilled person to apply this teaching to two cascaded PLLs.

2.8.4 It is generally known in the art that differential circuits can normally operate at higher speed and are less sensitive to noise than comparable single-ended circuits. It is thus evident to a skilled person that differential circuit architecture would be particularly advantageous in particular in the specific case of a circuit for generating a stabilized oscillation.

2.8.5 As to the alleged difficulty that the skilled person would face in applying this differential architecture to two cascaded PLL, it is noted that the differential receive circuit coupled with an input of the comparator of the second PLL unit has merely the task of converting the double-ended output of the oscillator of the first PLL unit to a single-ended output signal that must be referenced to the same level as the other input signal fed to the comparator. However, matching the output of a first circuit to an input of a second circuit is a routine problem that the skilled person is well equipped to solve.

2.8.6 Furthermore, D6 teaches that to *"further reduce PLL jitter due to power supply noise, the analog and digital PLL portions are wired to two separate die power- supply pads"* (D6, page 1259, left-hand column, bottom paragraph). In general, this implies that different portions of an integrated circuit should have separate power supplies in particular when they operate at different frequencies. The use of a separate power supply for each circuit or circuit portion implies, however, that each circuit output is effectively a differential signal referenced to the corresponding power supply. The application of the above teaching of

D6 to two cascaded PLLs would result in a circuit comprising a separate power supply for each PLL unit, a differential output circuit for the first PLL unit and a differential receive circuit for the second PLL unit.

2.8.7 Hence, the Board is of the opinion that, in the light of the teaching of D6 concerning the use of differential circuit architecture and of separate power sources in a PLL comprising a digital and an analog portion, it would be obvious to the person skilled in the art, facing the task of implementing the two cascaded PLLs known from D1, to arrive at a circuit comprising features (g) and (h).

2.9.1 As features (c) to (h) are essentially based on a straightforward application of the general knowledge common in the art of circuit design and of the teaching of D6, it would be obvious to a skilled person, wishing to implement the frequency generator known from D1, to arrive at a circuit falling within the terms of claim 1.

2.9.2 Hence, the subject-matter of claim 1 of the main request does not involve an inventive step within the meaning of Article 56 EPC.

First auxiliary request

3.1 Claim 1 according to the first auxiliary request differs from claim 1 of the main request in that it further comprises the following feature:

– *"a dedicated power source (23A, 23B) is provided for each of said unit circuits (20A, 20B)"*

3.2 As shown above, it is known for instance from D6 that PLL jitter due to power supply noise can be reduced by wiring the analogue and the digital portion of the PLL to two separate supply pads. The principle of using separate power sources for different circuits applied to the cascaded PLLs known from D1 leads to a frequency generator comprising the above feature.

3.3 For the above reasons, the subject-matter of claim 1 of the first auxiliary request does not involve an inventive step (Article 56 EPC).

Second auxiliary request

4.1 The second auxiliary request which was filed by fax on 7 September 2010, that is two days before the date of the oral proceedings, differs from the first auxiliary request in that claim 1 further contains the following feature:

– each of said unit circuits (20A, 20B) "*has substantially the same basic configuration and*".

4.2 In view of the very late filing of this request and of the fact that the amendment appears to raise new objections relating to its exact meaning and purpose in the context of the claimed subject-matter, the Board in the exercise of its discretion has decided not to admit the appellant's second auxiliary request into the appeal proceedings (Article 13(3) RPBA).

5. As none of the appellant's requests relates to patentable subject-matter, the application has to be refused.

Order

For the above reasons it is decided that:

The appeal is dismissed.

The Registrar: The Chairman:

U. Bultmann M. Ruggiu