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Case Number: T 0820/07 - 3.4.03

Application Number: 02001081.5

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Language of the proceedings: EN

Title of invention:
LCD and driving method thereof

Applicant:
SAMSUNG ELECTRONICS CO., LTD.

Opponent:
-

Headword:
-

Relevant legal provisions:
-

Relevant legal provisions (EPC 1973):
EPC Art. 54, 56

Keyword:
"Novelty (yes)"
"Inventive step (no)"

Decisions cited:
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Catchword:
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Case Number: T 0820/07 - 3.4.03

D E C I S I O N
of the Technical Board of Appeal 3.4.03
of 2 February 2010

Appellant: SAMSUNG ELECTRONICS CO., LTD.
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Decision under appeal: **Decision of the Examining Division of the European Patent Office posted 2 November 2006 refusing European application No. 02001081.5 pursuant to Article 97(1) EPC.**

Composition of the Board:

Chairman: G. Eliasson
Members: R. Q. Bekkering
T. Bokor

Summary of Facts and Submissions

I. This is an appeal against the refusal of application 02 001 081 for lack of novelty, Article 54(1) and (2) EPC 1973, (main request) over

D1: US 6 064 363 A,

and for lack of inventive step, Article 56 EPC 1973, (auxiliary request) over D1,

D2: JP 11 085 115 A, and

D6: US 5 892 493 A.

II. At oral proceedings before the board, the appellant applicant requested that the decision under appeal be set aside and that a patent be granted on the basis of claims 1 to 7 submitted during the oral proceedings.

III. Claim 1 reads as follows:

"A liquid crystal display comprising:
a liquid crystal panel (100) comprising a plurality of gate lines (G1-Gn), a plurality of insulated data lines (Dl-Dm) crossing the gate lines (G1-Gn), and a plurality of first thin film transistors (120) each having a gate electrode connected to a gate line, a source electrode connected to a data line, and a drain electrode connected to a liquid crystal capacitor (Cl);
a gate driver (200) for sequentially supplying a gate-on voltage to the gate lines (G1-Gn) for turning on the thin film transistors (120);

a data driver (300) for applying a data voltage to the data lines (D1-Dm), such that the polarities of the data voltages applied to the adjacent data lines (Dl-Dm) are opposite to each other, each said data voltage being a swing voltage with reference to a common voltage (Vcom) which is in the middle of the swing voltages;
a data line shared switch (400) having a plurality of switching devices (410), each of which formed between the adjacent data lines so as to short the adjacent data lines when the switching devices (410) are turned on; and
a shared signal generator (500, 900) for outputting a shared control signal (SH, SH1, SH2) for turning on the switching devices (410) to connect the adjacent data lines, characterized in that the data line shared switch (400) is placed at one end of the liquid crystal panel (100) opposite to the data driver (300), and in that each of the switching devices (410) is formed between all adjacent data lines, the shared signal generator (500) being suitable to apply a shared signal pulse for sharing the data lines (Dl-Dm) after the voltage applied to the previous gate lines turns to a gate-off voltage and before the gate-on voltage is applied to the gate line and, after the gate-on voltage is applied to the gate line, the shared signal pulse is maintained for a predetermined time."

IV. The appellant in substance provided the following arguments:

The display of document D6 was very different from the claimed display, so that D6 would not be considered relevant by the skilled person. In particular, D6

involved an arrangement of the data lines in groups with respective precharging circuitry, whereas the application was concerned with charge sharing between all data lines of the panel. Furthermore, the claimed timing of the gate-on voltage for the gate line and the gate-on voltage for the switching devices shorting the data lines provided for a more balanced charge redistribution. In contrast, the timing solution of D6 involved a simultaneous switching-on of the gate line and the switching devices for shorting the data lines, leading to unpredictable states. Accordingly, an inventive step had to be recognised for the subject-matter of claim 1.

Reasons for the Decision

1. The appeal is admissible.

2. *Novelty*

2.1 *Document D6*

2.1.1 Document D6 (cf figure 7) discloses a liquid crystal display comprising, using the terminology of claim 1, a liquid crystal panel comprising a plurality of gate lines (G1-Gm), a plurality of insulated data lines (d1A, d2A,..) crossing the gate lines, and a plurality of first thin film transistors (24) each having a gate electrode connected to a gate line, a source electrode connected to a data line, and a drain electrode connected to a liquid crystal capacitor (18) (cf figures 1 and 7; column 7, line 8 to column 10, line 35 and column 13, line 40 to column 15, line 49).

It is noted that in D6 (cf column 7, lines 24 to 50) the source and drain electrodes are interchanged with respect to claim 1. This difference, however, is merely definitional and does not provide any distinction in terms of structure or function.

Furthermore, the liquid crystal display of document D6 comprises a gate (line) driver (34) for sequentially supplying a gate-on voltage to the gate lines (G1-Gm) for turning on the thin film transistors (24) and a data (line) driver (40) for applying a data voltage to the data lines (d1A, d2A,..).

The display of D6 is for instance driven in the dot inversion mode (cf figure 4C, column 13, lines 52 to 59). As a result, the polarities of the data voltages applied to the adjacent data lines (Dl-Dm) are opposite to each other and "*each said data voltage being a swing voltage with reference to a common voltage which is in the middle of the swing voltages*" as per claim 1 (see also column 14, lines 37 to 47).

The liquid crystal display panel of document D6 also comprises a data line shared switch having a plurality of switching devices (42), "*each of which formed between all the adjacent data lines*" as per claim 1, so as to short the adjacent data lines when the switching devices are turned on (figures 7, 8B and column 13, line 52 to column 14, line 11). Furthermore, the display of D6 comprises a shared signal generator (44) for outputting a shared control signal (A, B,..) for turning on the switching devices (42) to connect the adjacent data lines (cf figure 3C).

In D6 the data line shared switch is placed at one end of the liquid crystal panel opposite to the data driver (40) (cf figure 7). Moreover, each of the switching devices is formed between all adjacent data lines.

It is noted that in the fourth embodiment of D6 referred to above (figure 7), the display transistors are divided in four groups and the switching devices short all adjacent data lines within one group. This stems from the fact that a fourfold multiplexing of the data line signal is used. However, a conventional driving system without multiplexing may be used instead (see also column 17, lines 34 to 38), in which case in substance only a single group (cf group A with data lines d1A, d2A,.. in figure 7) would be present in which all adjacent data lines of the display would be shorted by the switching devices.

2.1.2 As to the appellant's argument that in D6 a precharging of the data lines is used rather than a charge redistribution as is the case in the application, it is noted that the fourth embodiment addressed above (figure 7) in fact makes use of charge redistribution, like the application. In particular, in this embodiment charge is moved between adjacent data lines at opposite potentials, so that in substance a zero volt potential on all data lines is obtained (cf column 14, line 37 to column 15, line 19 and figures 7 and 8B). Like in the application, in case of a display driving mode with alternating positive and negative data line driving, this reduces the time required to charge the data lines and pixels with the required data voltage.

2.1.3 As shown in figures 3A and 3C of D6, the gate-on voltage for the switching devices (42) (ie the "*shared signal pulse*" of claim 1) shorting adjacent data lines of data line group A (pulse A in figure 3C) may be applied in the interval between gate-on signals (figure 3A) sequentially supplied to the TFT's of the gate lines.

It is noted that in the absence of any multiplexing, as discussed above, pulse A in figure 3C would short all adjacent data lines of the display.

This timing condition in fact corresponds in substance to the timing of the example, no longer falling within the terms of claim 1, shown in figure 5 of the application.

Furthermore, according to D6 it is preferable to advance the timing of the application of the gate voltage to the gate line as shown with dashed lines in figure 3A. Accordingly, the gate voltage is applied to the gate line when the gate-on voltage is applied to the switching devices (pulse A in figure 3C) (cf column 15, lines 20 to 24).

As a result, the charge accumulated between the electrode pair of the display connected to the data line is allowed to flow to the data line (and vice versa) so as to be included in the charge redistribution over all data lines, and substantially zero volt is obtained on all data lines and pixels (cf column 15, lines 20 to 49).

2.2 Claim 1, however, requires "*the shared signal generator being suitable to apply a shared signal pulse for sharing the data lines after the voltage applied to the previous gate lines turns to a gate-off voltage and before the gate-on voltage is applied to the gate line and, after the gate-on voltage is applied to the gate line, the shared signal pulse is maintained for a predetermined time*". It thus defines an "*intermediate*" signal timing, which lies between the two alternatives depicted in figures 3A and 3C of D6, discussed above.

This feature is not known from document D6 so that the subject-matter of claim 1 is new with respect to D6 (Article 54(1) and (2) EPC 1973).

2.3 The subject-matter of claim 1 is also new with respect to document D1, which differs in the location of the switch and the switching devices and in the timing of the gate-on voltage of the gate line and the charge sharing pulse (cf figures 5 and 7). It is furthermore new with respect to document D2, which discloses the claimed location of the switch and the switching devices but a different signal timing (cf figure 7).

3. *Inventive step*

3.1 The display of claim 1 in substance differs from that of D6 in that it provides an "*intermediate*" signal timing in which the gate-on signal for the gate line is advanced to a lesser extent than in figure 3A (dashed line) of D6.

According to D6, as discussed above, the reason for advancing the gate-on signal for the gate line with

respect to the gate-on voltage for the switching devices shorting adjacent data lines, is to allow the charge accumulated between the electrode pair of the display cell connected to the data line to flow to the data line (and vice versa) so as to be included in the charge redistribution over all data lines.

The time required for this charge flow will vary depending on the display characteristics, in particular the pixel capacitance, the pixel TFT characteristics etc.

3.2 Accordingly, the objective problem to be solved relative to D6 is to adapt the signal timing to a particular display with given characteristics and charge redistribution requirements.

The problem *per se* is obvious to a person skilled in the art of liquid crystal display technology, as the teaching of D6 is generally applicable to different displays.

Furthermore, although D6 shows a full advancing of the gate-on signal for the gate lines (dashed line in figure 3A) so as to substantially coincide with the gate-on signal for the switching devices (pulse A in figure 3C), it would be readily apparent to the skilled person that advancing of the gate-on signal for the gate lines is only required to such an extent that sufficient redistribution of charge between the display cell and the corresponding data line is achieved. Accordingly, it would be obvious to the skilled person to advance the gate-on signal for the gate lines in D6 to a lesser extent for a given display, provided that

adequate charge redistribution is achieved, thereby arriving at an "*intermediate*" signal timing as per claim 1.

3.3 The appellant argued that D6 merely disclosed two alternative solutions and contained no hint whatsoever for the claimed "*intermediate*" signal timing.

In the board's view, however, since document D6 contains a clear teaching as to the reason for advancing the gate-on signal, it provides guidance to the skilled reader for a purposive selection of timing conditions beyond the mere two alternative solutions shown in figure 3A and 3C.

Furthermore, the appellant argued that the occurrence of unpredictable states in the display circuit of D6 due to the simultaneous switching-on of the transistors of a gate line and the switching devices shorting the data lines would lead away from the claimed invention. Moreover, the appellant argued that a two-stage charge redistribution caused by the claimed "*intermediate*" timing would provide an unexpected and advantageous effect, indicative of the presence of an inventive step.

When the transistors of a gate line and the switching devices shorting the data lines are simultaneously switched, on the one hand each pixel capacitor addressed by the gate line is interconnected with the corresponding data line and thus charge flows therebetween, and on the other hand the data lines are interconnected (which are at opposite polarities) causing a corresponding charge redistribution.

The board is unable to see the occurrence of any unpredictable states under these conditions. As to the appellant's second argument, the two-stage discharge due to a later switching-on of the switching devices shorting the data lines as claimed, indeed delays the charge flow between pixel capacitor and data lines. There is, however, nothing advantageous or unexpected about this, so that no support for inventive step can be seen in this respect.

3.4 Accordingly, the subject-matter of claim 1 is obvious to a person skilled in the art and thus lacks an inventive step in the sense of Article 56 EPC 1973.

Order

For these reasons it is decided that:

The appeal is dismissed.

Registrar | Chair

S. Sánchez Chiquero | G. Eliasson