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Datasheet for the decision of 11 March 2010

Case Number: T 0563/07 - 3.5.02

Application Number: 00308382.1

Publication Number: 1091494

IPC: H03M 1/56

Language of the proceedings: EN

Title of invention:
Analog to digital converter using asynchronously swept thermometer codes

Applicant:
LUCENT TECHNOLOGIES INC.

Opponent:
-

Headword:
-

Relevant legal provisions:
EPC Art. 54

Relevant legal provisions (EPC 1973):
-

Keyword:
"Lack of novelty - yes"

Decisions cited:
-

Catchword:
-

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Beschwerdekammern | Boards of Appeal | Chambres de recours

Case Number: T 0563/07 - 3.5.02

D E C I S I O N
of the Technical Board of Appeal 3.5.02
of 11 March 2010

Appellant: Lucent Technologies, Inc.
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Representative: Williams, David John
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Decision under appeal: **Decision of the Examining Division of the European Patent Office posted 9 November 2006 refusing European patent application No. 00308382.1 pursuant to Article 97(1) EPC 1973.**

Composition of the Board:

Chairman: M. Ruggiu
Members: J.-M. Cannard
P. Mühlens

Summary of Facts and Submissions

I. The appellant contests the decision of the examining division of 9 November 2006 to refuse European patent application No. 00 308 382.1. The reason given for the refusal was that the subject-matter of the then claim 1 was not new (Article 54(1) and (2) EPC) and the subject-matter of the then independent claim 14 did not involve an inventive step (Article 56 EPC).

II. The prior art document:

D2: FR-A-2 749 456,

considered in the first instance, remains relevant to the present appeal.

III. A communication of the Board dated 11 December 2009 annexed to summons to oral proceedings indicated that the method set out in independent claim 8 filed with the statement of grounds of appeal appeared to lack novelty in view of document D2.

IV. With a letter dated 28 January 2010, the appellant withdrew their request for oral proceedings and requested that a decision be taken on the basis of the file as it currently stands.

V. The appellant did not attend the oral proceedings before the Board which were held on 11 March 2010. It can be understood from the file as it stands that the appellant requests that the decision under appeal be set aside and that a patent be granted on the basis of an amended set of claims 1 to 10 filed with the

statement of grounds of appeal in a letter dated 16 March 2007.

VI. Independent claim 8 filed with the statement of grounds of appeal reads as follows:

"8. A method for generating a ramp voltage for comparison with an analogue voltage to be digitized, comprising the following steps:
providing a plurality of clock pulses;
using a chain of buffers to provide a first signal at each successive clock pulse;
providing a sample of an analog input voltage occurring at each clock pulse;
providing a reference voltage;
dividing the reference voltage into at least two contiguous ranges;
deriving a second signal indicating the voltage ranges exceeded by the voltage sample;
combining the second signal with the first signal to generate a binary digital signal;
generating a ramp voltage corresponding to the binary digital signal, wherein the ramp voltage increases as the binary digital signal increases;
comparing the amplitude of the ramp voltage to the amplitude of the analog input voltage;
producing an output signal from the comparing step when the analog voltage and the ramp voltage have the same amplitude;
freezing the amplitude of the ramp voltage in response to the output signal; and
converting the binary digital signal at the time of the freezing into a binary digital representation of the analog input voltage.; and (*sic*)"

VII. The appellant's arguments can be summarized as follows:

Independent claim 8 recited the method counterpart of figure 2 of the application, where a thermometer code was generated by combining the outputs of comparators 68 to 74 with the output of buffers 14 to 18. This method improved the resolution of the thermometer code without adding more buffer elements or requiring clock pulses to propagate through the entire buffer chain of the means for generating the thermometer code. The subject-matter of claim 8 involved an inventive step over the teachings of documents D1 (DE-B-2 346 010) and D2 taken in combination. There was no way to improve the resolution of the output in D1 without adding display elements and buffer chain elements. The structure of D1 did not lend itself to the incorporation of elements, such as those described in D2, that might be employed to improve resolution of the digital to analog conversion.

Reasons for the Decision

1. The appeal is admissible.

2. Document D2 discloses (figures 3 to 5; table 1; page 6, line 6 to page 7, line 21) an apparatus which performs a method (page 8, line 5 to page 9, line 31) for generating a ramp voltage for comparison with an analog input voltage to be digitized that comprises all the features recited in the independent method claim 8, namely:

providing a plurality of clock pulses (CLK1);

using a chain of buffers to provide a first signal (less significant bits of Q0 to Q7 in counter 32) at each successive clock pulse, because the counter 32 implicitly includes a chain of buffers to provide an output signal at each successive clock pulse;

providing a sample of an analog input voltage (IN) occurring at each clock pulse;

providing a reference voltage V_{REF};

dividing the reference voltage into at least two contiguous ranges (R1 to R16);

deriving a second signal indicating the voltage ranges exceeded by the voltage sample (figure 3, 31; figure 4, $CP4_1$ to $CP4_{16}$; 41: Q0 to Q3; 42: D0 to D7);

combining the second signal with the first signal to generate a binary digital signal (counter 32; Q0 to Q7);

generating a ramp voltage corresponding to the binary digital signal, wherein the ramp voltage increases as the binary digital signal increases (D/A converter 2);

comparing the amplitude of the ramp voltage to the amplitude of the analog input voltage (CP1);

producing an output signal from the comparing step when the analog voltage and the ramp voltage have the same amplitude (CP1 output signal);

freezing the amplitude of the ramp voltage in response to the output signal (AND gate ET1; see pages 3 and 4, bridging paragraph); and

converting the binary digital signal (Q0 to Q7) at the time of the freezing into a binary digital representation of the analog input voltage (latch 3 which corresponds to latch 50 of the application).

3. Since D2 discloses a method for generating a ramp voltage for comparison with an analog input voltage to be digitized which comprises all the features recited in the current independent method claim 8, the subject-matter of claim 8 is not new (Article 54 EPC).

4. Since the application does not meet the requirements of the EPC, the appeal has to be dismissed.

Order

For these reasons it is decided that :

The appeal is dismissed.

The Registrar: The Chairman:

U. Bultmann M. Ruggiu