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Datasheet for the decision of 6 October 2009

Case Number: T 0322/07 - 3.4.03

Application Number: 98960430.1

Publication Number: 1034563

IPC: H01L 21/311

Language of the proceedings: EN

Title of invention:
High selectivity etching process for oxides

Applicant:
Micron Technology, Inc.

Opponent:
-

Headword:
-

Relevant legal provisions:
-

Relevant legal provisions (EPC 1973):
EPC Art. 56

Keyword:
"Inventive step (yes) - after amendment"

Decisions cited:
-

Catchword:
-

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Beschwerdekammern | Boards of Appeal | Chambres de recours

Case Number: T 0322/07 - 3.4.03

D E C I S I O N
of the Technical Board of Appeal 3.4.03
of -

Appellant: Micron Technology, Inc.
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Representative: Caldwell, Judith Margaret
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Decision under appeal: **Decision of the Examining Division of the European Patent Office posted 5 September 2006 refusing European application No. 98960430.1 pursuant to Article 97(1) EPC.**

Composition of the Board:

Chairman: G. Eliasson
Members: R. Q. Bekkering
P. Mühlens

Summary of Facts and Submissions

I. This is an appeal against the refusal of application 98 960 430 for lack of inventive step (main request) and added subject-matter (auxiliary request).

II. The appellant applicant requested that the decision under appeal be set aside and a patent granted on the basis of the following documents:

Main request:

Claims: Claims 1 to 10 filed with letter dated 17 September 2009;
Description: Pages 1 and 5 to 9 as originally filed;
Page 2 filed with letter dated 7 September 2009;
Pages 3 and 4 filed with letter dated 17 September 2009;
Drawings: Sheets 1/3 to 3/3 as originally filed (and published).

First auxiliary request:

Claims: Claims 1 to 5 filed with letter dated 15 January 2007.

Second auxiliary request:

Claims: Claims 1 to 5 filed with letter dated 15 January 2007.

III. Claims 1 and 6 according to the main request read:

"*1. A process for etching comprising the steps of:*
providing a substrate (10; 20) having a surface wherein the surface of said substrate (10; 20) includes a first silicon oxide layer (12; 22) on a portion thereof and a second silicon oxide layer (14) directly overlying said first silicon oxide layer (12; 22), said first silicon oxide being relatively more dense than said second silicon oxide, and
exposing said second oxide layer (14) to an etchant for said second oxide layer (14), characterized in that said etching process is carried out by first exposing said second oxide layer (14) to an aqueous solution of hydrofluoric acid to remove an upper portion of said second oxide layer (14) to leave a remaining portion such that said first oxide layer (12; 22) is not exposed, followed by exposing said second oxide layer (14) to a gas phase comprising a halide-containing species to remove the remaining portion of said second oxide layer (14), wherein the step of exposing said second oxide layer (14) to said gas phase causes said second silicon oxide to selectively etch at a greater rate than the etch of said first silicon oxide.

6. A process for forming a capacitor storage cell on a semiconductor substrate (10; 20) comprising the steps of:
forming a first layer (12; 22) of a silicon oxide on the surface of said substrate (10; 20);
forming a second layer (14) of a silicon oxide directly on said first layer of silicon oxide (12; 22), said first silicon oxide layer being relatively more dense than said second silicon oxide layer; forming an

opening into said first and second silicon oxide layers (12, 14; 22);
forming a polysilicon or amorphous silicon container structure (16; 23) having generally vertically-oriented side walls (17) in said opening;
exposing said second silicon oxide layer (14) to an etchant to expose the side_walls (17) of said container structure (16; 23), without exposing said substrate (10; 20) to oxygen or an oxygen-containing gas, annealing said container walls (17) at an elevated temperature to transform said polysilicon or amorphous silicon into hemispherical grain silicon;
conductively doping said hemispherical grain silicon walls (17) to form capacitor plates;
forming a capacitor dielectric layer over said capacitor plates; and
forming a second conductive silicon layer over said capacitor dielectric layer, characterized in that the step of exposing said second silicon oxide layer (14) to an etchant to expose the side_walls (17) of said container structure (16; 23) comprises:
removing an upper portion of said second silicon oxide layer (14) to leave a remaining portion by exposing said second silicon oxide layer (14) to an aqueous solution of hydrofluoric acid such that said first silicon oxide layer (12; 22) is not exposed; and
selectively removing the remaining portion of said second silicon oxide layer (14) by exposing said second silicon oxide layer (14) to a gas phase comprising a halide-containing species".

IV. The following prior art documents are referred to:

D5: EP 0 704 884 A

D7: US 5 340 765 A

V. The appellant applicant argued as follows:

The subject-matter of claim 1 involved an inventive step with respect to document D5. Document D5 provided a different structure to be etched and there was nothing suggesting the skilled person to modify this structure. Moreover, the skilled person would not modify the etching process of D5 by including a fast non-selective etching process. Firstly, there was nothing in D5 suggesting that etching speed was an issue and thus that an increase thereof was desirable. Furthermore, there was nothing in D5 suggesting abandoning the selectivity required in D5. Having regard to document D7, disclosing the features of the pre-characterising portion of claim 1 (and 6), there was no suggestion that a skilled person would modify the process to arrive at a two-stage etching process as claimed.

Reasons for the Decision

1. The appeal is admissible.

2. *Main request*

2.1 *Amendments*

Claim 1 is based on claims 1, 4 and 6 as originally filed and on the description as originally filed

(page 5, line 22 to page 6, line 5; page 6, lines 13 to 21; page 6, line 28 to page 7, line 2).

Dependent claims 2 to 5 are based on original claims 2, 3, 5 and 8, respectively.

Claim 6 is based on claim 17 as originally filed and on page 6, lines 13 to 21 of the description as originally filed.

Dependent claims 7 to 10 are based on original claims 18 to 21, respectively.

The amendments thus comply with Article 123(2) EPC.

2.2 *Novelty*

2.2.1 *Document D5*

Document D5 discloses a process for etching a porous silicon oxide layer selectively with respect to a dense silicon oxide layer. In particular, the etching process is used to build a cylindrical capacitor in a semiconductor device. In the manufacturing process a silicon wafer 10 is provided with a dense blanket layer of TEOS silicon oxide 12 (cf page 4, lines 31 to 37 and figure 1). On layer 12, a polysilicon cylinder 14, comprising bottom member 16 and side wall 18 has been built up. The manufacturing process has left cylinder 14 filled with porous BP TEOS silicon oxide layer 20. TEOS layer 12 is in the range of 3000 Å. The thickness of the BP TEOS layer 20 is generally in the range of 4,000 Å - 7,000 Å, typically 4,500 - 5,000 Å. The process for removing layer 20 must achieve a removal of

about 5,000 Å BP TEOS while removing less than 100 Å of adjacent TEOS so as to avoid undue undercutting of the cylinder.

In document D5 the first oxide layer 12 underlying the second oxide layer 20, in the portion thereof adjacent the cylinder 14, is exposed to the etching process of the second oxide layer 20 from the start, thereby making a high selectivity necessary.

In the etching process of document D5 there is no first etching step using an aqueous solution of hydrofluoric acid as per claim 1.

Moreover, according to claim 1 during the first part of the etching process in which the second oxide is exposed to an aqueous solution of hydrofluoric acid, the first oxide layer is not exposed.

Furthermore, according to claim 1 as amended the second silicon oxide layer is formed directly overlying the first, relatively more dense silicon oxide layer.

The subject-matter of claim 1 is accordingly new over document D5 (Article 54(1) and (2) EPC 1973).

The above also applies, *mutatis mutandis*, to the subject-matter of claim 6. Furthermore, the remaining claimed process steps of forming the capacitor storage cell are not known from D5.

2.2.2 *Document D7*

Document D7 discloses a process of forming a container capacitor in a semiconductor device. In particular, the process comprises the steps of forming a first layer of a silicon oxide (14) on the surface of the substrate and then forming a second layer of a silicon oxide (16) on the first layer of silicon oxide, with the first silicon oxide (eg TEOS) being relatively more dense than the second silicon oxide (eg BPSG) (column 2, line 58 to column 3, line 6; column 4, lines 17 to 26; figure 1). An opening is formed into the first and second silicon oxide layers, and a polysilicon or amorphous silicon container structure is formed having generally vertically-oriented side walls in the opening (column 3, line 28 to column 4, line 6 and figures 2A to 5). The second silicon oxide layer is selectively removed by exposing the second silicon oxide layer to a wet oxide etch back, thereby exposing the side walls of the container structure (column 4, lines 12 to 26 and figure 6). Without exposing the substrate to oxygen or an oxygen-containing gas, the container walls are annealed at an elevated temperature to transform the polysilicon or amorphous silicon into hemispherical grain silicon (column 4, lines 27 to 45 and figures 7A, 7B). The hemispherical grain silicon walls are conductively doped to form capacitor plates (implicit), and a capacitor dielectric layer is formed over the capacitor plates (column 4, lines 46 to 47 and figure 8). Finally, a second conductive silicon layer is formed over the capacitor dielectric layer to complete the structure (column 4, lines 47 to 50 and figure 8).

Accordingly, document D7 discloses a process of forming a capacitor storage cell with corresponding etching process as provided in the application description as originally filed (page 4, lines 2 to 19) and according to the pre-characterising portion of independent claims 1 and 6 of the main request.

However, whereas D7 uses a wet oxide etch back to remove the second silicon oxide layer, according to claims 1 and 6 the etching process for removing the second silicon oxide layer consists of two steps:

a first step of exposing the second silicon oxide layer to an aqueous solution of hydrofluoric acid, to remove an upper portion of the second silicon oxide layer and to leave a remaining portion, so that the first silicon oxide layer underlying the second silicon oxide layer is not exposed, and

a second step of exposing the second silicon oxide layer to a gas phase comprising a halide-containing species to selectively remove the remaining portion of the second silicon oxide layer.

Accordingly, the subject-matter of claims 1 and 6 is also new over document D7 (Article 54(1) and (2) EPC 1973).

2.2.3 The subject-matter of claims 1 and 6 is also new over the remaining available, more remote prior art.

2.3 *Inventive step*

2.3.1 *Document D5*

In the decision under appeal, document D5 was considered the closest prior art.

The process according to claim 1 differs from D5 in that it has a first etching step using an aqueous solution of hydrofluoric acid.

However, the fact that in document D5 the first silicon oxide layer adjacent the cylinder is exposed to the etching process from the start, precludes the use of a first etching step using an aqueous solution of hydrofluoric acid as in the process of claim 1, as this etching solution is generally unselective and thus would undesirably remove a substantial portion of this layer.

Furthermore, claim 1 requires that the first oxide layer is not exposed during the first step of the etching process in which the second oxide layer is exposed to an aqueous solution of hydrofluoric acid. Moreover, the second silicon oxide layer is formed directly overlying the first, relatively more dense silicon oxide layer.

In order to arrive at both these features of claim 1, modifications of the structure subjected to the etching process in D5 would be required. Firstly, the first silicon oxide layer in the portion adjacent the cylinder would have to be covered. Secondly, the bottom member 16 would have to be eliminated. There is however

nothing in D5 or elsewhere suggesting such modifications.

Accordingly, starting from document D5 the subject-matter of claim 1 would not be obvious to a person skilled in the art.

This is all the more true for the subject-matter of claim 6 as the remaining claimed process steps of forming the capacitor storage cell are not known from D5.

2.3.2 *Document D7*

Document D7 provides in the board's judgement the closest prior art, as it discloses the same structure as that subjected to the etching process in claims 1 and 6.

According to D7 the wet oxide etch back process used has a much higher etch rate for BPSG (layer 16) compared to TEOS (layer 14). The etch process is thus considered to be sufficiently selective.

Even if the skilled person would wish to improve on the etch selectivity and refer to document D5 to this end, he would not arrive at the two step etching process as per claims 1 and 6. In this case he would merely replace the wet oxide etch back of D7 by the highly selective gas phase etching process of D5. As discussed above, document D5 leads away from adding a preliminary etching step using an aqueous solution of hydrofluoric acid, as this would not be possible in the structure of D5. Furthermore, there is nothing in D5 or D7, or in

any other available prior art, suggesting to use of an initial wet etch to more rapidly remove the porous oxide without being concerned about selectivity, followed by a selective etching process once it becomes likely that the more dense oxide will be exposed.

Accordingly, the subject-matter of claims 1 and 6, having regard to the available state of the art, is not considered to be obvious to the person skilled in the art and, thus, involves an inventive step (Article 56 EPC 1973).

2.4 Claims 2 to 5 and 7 to 10 are dependent on claims 1 and 6, respectively, providing further limitations. The subject-matter of these claims, therefore, also involves an inventive step.

3. The patent application amended in accordance with the appellant's main request also meets the remaining requirements of the EPC, so that a patent can be granted on the basis of these documents.

4. As a consequence there is no need to go into the merits of the appellant's auxiliary requests.

Order

For these reasons it is decided that:

1. The decision under appeal is set aside.

2. The case is remitted to the department of the first instance with the order to grant a patent in the following version:

Claims:	Claims 1 to 10 filed with letter dated 17 September 2009;
Description:	Pages 1 and 5 to 9 as originally filed; Page 2 filed with letter dated 7 September 2009; Pages 3 and 4 filed with letter dated 17 September 2009;
Drawings:	Sheets 1/3 to 3/3 as originally filed (and published).

Registrar: Chair:

S. Sánchez Chiquero G. Eliasson