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Datasheet for the decision of 4 February 2010

Case Number: T 0185/07 - 3.5.02

Application Number: 00930753.9

Publication Number: 1177620

IPC: H03F 3/45

Language of the proceedings: EN

Title of invention:
Compensation mechanism for compensating bias levels of an operation circuit in response to supply voltage changes

Applicant:
HONEYWELL INC.

Opponent:
-

Headword:
-

Relevant legal provisions:
EPC Art. 56

Relevant legal provisions (EPC 1973):
-

Keyword:
"Inventive step (no)"

Decisions cited:
-

Catchword:
-

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Beschwerdekammern | Boards of Appeal | Chambres de recours

Case Number: T 0185/07 - 3.5.02

D E C I S I O N
of the Technical Board of Appeal 3.5.02
of 4 February 2010

Appellant: HONEYWELL INC.
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Decision under appeal: **Decision of the Examining Division of the European Patent Office posted 29 September 2006 refusing European application No. 00930753.9 pursuant to Article 97(1) EPC 1973.**

Composition of the Board:

Chairman: M. Ruggiu
Members: J.-M. Cannard
E. Lachacinski

Summary of Facts and Submissions

I. The appellant contests the decision of the examining division of 29 September 2006 to refuse European patent application No. 00 930 753.9.

II. The decision under appeal is based on amended independent claims 1 and 7 filed with a letter of 19 July 2005. According to a communication from the examining division dated 22 February 2006, to which the appealed decision refers, the subject-matter of claims 1 and 7 lacks an inventive step, Article 56 EPC.

III. The prior art document:

D5: EP-A-0 426 594,

considered in the first instance, remains relevant to the present appeal.

IV. Oral proceedings before the Board were held on 4 February 2010. As announced in a letter dated 11 November 2009, the appellant did not attend the oral proceedings. He had requested in writing that the decision under appeal be set aside and that a patent be granted on the basis of the claims filed with the letter dated 19 July 2005.

V. Independent claims 1 and 7 filed with the letter of 19 July 2005 read as follows:

"1. An operational circuit and compensation circuit combination, the compensation circuit for providing compensation to the operational circuit in response to

variations in a supply voltage, the operational circuit having a number of devices connected in a predetermined manner via a number of circuit nodes, a selected circuit node having a voltage that is dependent on the supply voltage, the compensation circuit comprising:

reference voltage generating means for generating a predetermined reference voltage that is relatively independent of the variations in the supply voltage;

comparing means coupled to said reference voltage generating means for comparing the reference voltage to the voltage of the selected circuit node; and

compensating means coupled to said comparing means for providing the operational circuit such that the voltage at the selected circuit node assumes a predetermined value relative to the reference voltage, characterised in that the reference voltage generating means comprises:

current source means for providing a current that is relatively independent of the variations in the supply voltage; and

current-to-voltage converter means coupled to said current source means for converting the current generated by the current source means to the reference voltage,

the operational circuit includes an amplifier having a differential pair of transistors and a current source transistor, wherein the current source transistor has a drain that is connected to a source of each of the differential pair of transistors."

"7. A method for providing compensation to an operational circuit in response to variations in a supply voltage, the operational circuit having a number of devices connected in a predetermined manner via a number of circuit nodes, a selected circuit node having a voltage that is dependent on the supply voltage, and including an amplifier having a differential pair of transistors and a current source transistor, wherein the current source transistor has a drain that is connected to a source of each of the differential pair of transistors, the method comprising the steps of:

generating a reference voltage that is relatively independent of the variations in the supply voltage;

comparing the reference voltage to the voltage of the selected circuit node; and

providing compensation to the operational circuit such that the voltage at the selected circuit node assumes a predetermined value relative to the reference voltage;

characterised in that the generating steps including the steps of:

providing a current that is relatively independent of the variations in the supply voltage; and

converting the current generated by the current providing step to the reference voltage."

VI. The appellant's arguments can be summarized as follows:

The subject-matter of present claims 1 and 7 involved an inventive step over the teaching of document D5.

FET and BJT transistors were not functional equivalents. Each type of device affected the type of circuit which included it in a different way, this difference being fundamental to the underlying concept of the present invention. FET devices were advantageous over BJT devices in the combination of circuits of the present invention because a FET gate was controlled by a voltage, while a BJT base was controlled by a current. In the circuit of D5, BJT devices required relatively high base currents and hence the accuracy of the reference voltage could not be guaranteed. This problem was solved by the use of FET devices in which the application of a voltage between the gate and source controlled the current flowing between the drain and source.

The substitution of a BJT for a FET in the circuits of the invention was not obvious. Even if FET and BJT devices were well known, their respective advantages in the particular field of the invention were not fully understood at the priority date of D5, nor at the priority date of the invention, as evidenced by the lack of relevant prior art cited. There was no mention or even suggestion in D5 that a FET device could be employed. No other prior art had suggested such a use for FET devices. The solution recognized by the claimed invention would not be apparent to those skilled in the art considering D5 alone.

Reasons for the Decision

1. The appeal is admissible.

2. Claim 1 of the current request relates to an operational circuit and compensation circuit combination which is a generalisation, *inter alia*, of the embodiment described in the application in suit with reference to figure 4. According to this embodiment, a reference voltage generating means 302 generates a predetermined reference voltage 326 that is relatively independent from the variations in the supply voltage 318. The reference voltage generating means 302 comprises current source means 303 and reference diodes 305 forming current-to-voltage converter means coupled to the current source means for converting the current generated by the current source means to the reference voltage 326 (see published application WO 00/70756, pages 19 and 20, bridging paragraph, and page 28, lines 13 to 23; figure 4 (302, 303, 305)). Therefore, claim 1 covers an operational circuit and compensation circuit combination in which the reference voltage generating means comprises a current source and reference diodes coupled to said source for converting the current generated by said source to a reference voltage that is relatively independent of the variations in the supply voltage.

3. The circuit combination set out in claim 1 does not involve an inventive step having regard to document D5 and the common general knowledge of the skilled person (Article 56 EPC).

3.1 With reference to figure 5 of D5 (column 4, line 19 to column 5, line 41) discloses an operational circuit (10)

and compensation circuit (16, 36) combination in which the compensation circuit provides compensation to the operational circuit 10 in response to variations in a supply voltage. The operational circuit has a number of devices (Q1, Q2, Q4, RE, RC, RBLG) connected in a predetermined manner via a number of circuit nodes, a selected circuit node (12, RBLG) having a voltage that is dependent on the supply voltage. The compensation circuit comprises:

reference voltage generating means (36) for generating a predetermined reference voltage;

comparing means (16) coupled to said reference voltage generating means (36) for comparing the reference voltage to the voltage of the selected circuit node (12); and

compensating means (Q3) coupled to said comparing means for providing the operational circuit (10) such that the voltage at the selected circuit node (12) assumes a predetermined value relative to the reference voltage,

wherein the reference voltage generating means comprises:

current source means (40) for providing a current; and

current-to-voltage converter means (D1, D2) coupled to said current source means for converting the current generated by the current source means to the reference voltage,

the operational circuit (10) including an amplifier having a differential pair of bipolar transistors (Q1, Q2) and a current source bipolar transistor (Q4).

3.2 The symbols 303 in figure 4 of the present application and 40 in figure 5 of D5 both correspond to the symbol which is conventionally used to represent an ideal current source, namely a current source which provides a current independent of any other variable (in particular the voltage supply) of the circuit that includes the current source. A physical current source cannot be made totally independent of the supply voltage of the circuit in which it is used and thus can be seen as providing a current relatively independent of the variations of the supply voltage, taking into account the vague meaning of the term "relatively independent". Moreover, claim 1 specifies reference voltage generating means for generating a predetermined reference voltage, that is relatively independent of the variations in the supply voltage in general terms which cover the examples of the reference voltage generating means referred to in the present application (see *supra* point 2). Accordingly, the Board considers that the voltage reference generating means specified in claim 1 and the voltage reference generating means 36 shown in figure 5 of D5, which have the same structure, both provide a reference voltage that is relatively independent of the variations of the voltage supply.

4. In view of the foregoing, the subject-matter of claim 1 differs from the circuit combination shown in figure 5 of D5 only in that the transistors of the operational circuit are FET transistors in claim 1 while the

operational circuit of figure 5 of D5 comprises bipolar transistors Q1, Q2 and Q4.

5. The Board judges that, at the priority date of the application in suit, the skilled person aware of the circuit of figure 5 of D5 would have considered using FET transistors instead of bipolar transistors, because it was generally known that FETs could frequently be used in place of bipolar transistors provided values of components in the circuit are adapted. Moreover, the skilled person aware of the circuits of D5 would have considered using FET transistors instead of bipolar transistors to benefit from the specific known advantages provided by FET devices, as a gate controlled by a voltage. Doing so, the skilled person starting from D5 would provide in an obvious way an operational circuit wherein the current source transistor has a drain that is connected to a source of each of the differential pair of transistors, as recited in current claim 1. Accordingly, claim 1 does not involve an inventive step (Article 56 EPC).

6. The same considerations apply to independent claim 7 which relates to a method for providing compensation to an operational circuit which corresponds, in terms of steps, to the circuit combination according to claim 1.

7. Since the application does not meet the requirements of the EPC, the appeal has to be dismissed.

Order

For these reasons it is decided that:

The appeal is dismissed.

The Registrar: The Chairman:

U. Bultmann M. Ruggiu