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Datasheet for the decision of 19 May 2010

Case Number: T 0137/07 - 3.5.02

Application Number: 02804002.0

Publication Number: 1446887

IPC: H03M 9/00

Language of the proceedings: EN

Title of invention:
Method of transferring data

Patentee:
Interdigital Technology Corporation

Opponent:
-

Headword:
-

Relevant legal provisions:
EPC Art. 54

Relevant legal provisions (EPC 1973):
-

Keyword:
"Novelty - no"

Decisions cited:
-

Catchword:
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Beschwerdekammern | Boards of Appeal | Chambres de recours

Case Number: T 0137/07 - 3.5.02

D E C I S I O N
of the Technical Board of Appeal 3.5.02
of 19 May 2010

Appellant: INTERDIGITAL TECHNOLOGY CORPORATION
Suite 527
300 Delaware Avenue
Wilmington, DE 19801 (US)

Representative: Henningsson, Gunnar
AWAPATENT AB
Box 45086
S-104 30 Stockholm (SE)

Decision under appeal: **Decision of the Examining Division of the European Patent Office posted 1 August 2006 refusing European patent application No. 02804002.0 pursuant to Article 97(1) EPC 1973.**

Composition of the Board:

Chairman: M. Ruggiu
Members: G. Flyng
E. Lachacinski

Summary of Facts and Submissions

I. The applicant appealed against the decision of the examining division refusing the European patent application no. 02 804 002.0.

II. The examining division refused the application on the grounds that claim 1 filed with the letter of 20 June 2006 lacked novelty, Article 54 EPC, in view of the following document:

D1: "Virtex SelectLink Communications Channel", John Logue, Xilinx Application Note XAPP234 (v1.1), 15 March 2000.

III. The appellant filed an amended set of claims 1 to 6 with the statement of grounds of appeal and argued that claim 1 was novel and inventive over document D1.

IV. The Board summoned the appellant to attend oral proceedings. In an annex to the summons the Board raised questions as to whether certain amendments to the claims were allowable under Article 123(2) EPC. Furthermore, the Board made observations on the patentability of claim 1 filed with the statement of grounds of appeal, in particular novelty with respect to document D1 and inventive step with respect to D1 and the following document:

D2: "Eight Channel, One Clock, One Frame LVDS Transmitter/Receiver", Ed McGettigan, Xilinx Application Note XAPP245 (v1.1), 15 March 2001.

V. With a letter dated 8 April 2010 the appellant filed an amended set of claims 1 to 7.

VI. Oral proceedings were held before the Board on 19 May 2010. The appellant requested that the decision under appeal be set aside and a patent be granted on the basis of claims 1 to 7 filed with the letter dated 8 April 2010.

VII. Independent claim 1 reads as follows:

"1. A method for determining a number of i bus connections required to transfer block data over a bus, each block of the block data having N number of bits wherein a demultiplexer is configured to demultiplex each block of N bits to i nibbles for serial transfer over i data transfer lines, each nibble being transferred over a given one of said transfer lines, the method comprising:

determining a maximum latency allowed for transfer of the block data;

determining a minimum number of connections required to transfer the data block with the maximum latency wherein each connection is configured to transfer one of the nibbles to its given one of the transfer lines in serial fashion by a parallel serial converter; and

determining i with i being a value at least the minimum number of required connections."

Claims 2 to 7 are dependent on claim 1.

VIII. The appellant argued essentially that the claims as amended did not introduce fresh subject-matter contrary to Article 123(2) EPC and were novel over document D1, Article 54 EPC.

In particular, D1 did not disclose dividing a data block into smaller groups of bits which each are transferred in a serial fashion by a parallel serial converter, the number of smaller groups corresponding to the number of converters. Furthermore, in D1 the data forming each nibble was spread across all of the transfer lines, whereas according to claim 1 each nibble was transferred over a given one of the transfer lines.

Reasons for the Decision

1. The appeal is admissible.

2. *Amendments, Article 123(2) EPC*

Independent claim 1 is based generally on independent claim 12 as filed and the amendments that have been made are derivable from the application as filed, see in particular WO 03/047113, paragraph [0045], third sentence.

For these reasons the Board finds that the amendments according to present claim 1 do not contravene Article 123(2) EPC.

3. *Novelty, Article 54 EPC*

3.1 Document D1 describes a Virtex SelectLink Communications Channel which, according to the summary on page 1, "*utilizes special features of the Virtex™ series of FPGAs including Delay Locked Loops (DLL), block SelectRAM+™ memory, and the SelectI/O™ interface, to create a system to move large amounts of data between FPGAs at very high speeds*".

Figure 4 on page 5 shows two such Virtex FPGAs, a transmitter and a receiver, connected via a SelectLink channel that is implemented by a transmit module SLXtc in the transmitter FPGA and a receive module SLRtc in the receiver FPGA. In the transmitter FPGA data is fed to the transmit module SLXtc via data bus SLx[m:0]. Data is transferred from the transmit module SLXtc to the receive module SLRtc via a double data rate data bus SL[n:0] (see also table 2 on page 4).

Figure 5 shows the transmit module SLXtc in more detail, with a funneling FIFO and one or more Cnvt2Dbl1, 2 or 4 modules. According to the description of figure 5: "*Words read from the FIFO are converted to double data rate with module Cnvt2DblN, where N is 1, 2, or 4. N is the width of the module output bus. For example, module Cnvt2Dbl4 converts an 8-bit byte to a double data rate 4-bit nibble by multiplexing the lower and upper nibbles, in that order, at the 2x clock rate. Multiple copies of the same Cnvt2DblN module are used to span the full width of the bus*".

From this disclosure it is evident to the skilled reader that each Cnvt2DblN module receives and converts

an 8-bit byte of the input data. Furthermore, in the case where D1 uses multiple Cnvt2Dbl1 modules (i.e. N = 1), each Cnvt2Dbl1 module would transmit its 8-bit byte serially at 2x clock rate on its 1-bit module output bus and n + 1 modules would be required to span the full width of the double data rate data bus SL[n:0].

3.2 The data fed into the input bus SL[m:0] of D1 represents a block of N bits in the sense of present claim 1, with N here being equal to m + 1.

Furthermore, the multiple Cnvt2DblN modules of D1 form a demultiplexer that demultiplexes (i.e. splits) each block of N = m + 1 bits into 8-bit bytes, one of which is handled by each Cnvt2DblN module. Being smaller parts of the input data block, these 8-bit bytes may be considered as "nibbles" in the broad sense of the word.

In the case where D1 uses multiple Cnvt2Dbl1 modules, each module has a 1-bit output bus, so the width of the double data rate data bus SL[n:0] must be the same as the number of Cnvt2Dbl1 modules.

Thus, in the terminology of claim 1 it may be said that document D1 discloses a demultiplexer that is configured to demultiplex each block of N = m + 1 bits into i nibbles (8-bit bytes) for serial transfer over i data transfer lines, where i corresponds to the number of Cnvt2DblN modules required in D1.

3.3 According to document D1, the Selectlink channel has the notable feature that "*the width of the internal FIFO ports and the width of the external inter-chip bus*

can be configured to match the design requirements" (see page 2, "Configurable Bus Widths").

In the section "Latency" on page 10 of D1 it is explained that latency, defined as the number of periods between the time a datum is written on the SLx bus and the time it appears on the SLr bus, is a function of the ratio of the internal and external bus widths, and the propagation time of the external bus. The relationship between latency and bus width ratio is set out in table 8. Table 8 thus enables the designer to determine the bus width ratio that will be required to achieve a given latency, expressed in clock periods. Given that the internal bus width (i.e. the width of the input data) will be fixed by the input data block, the bus width ratio enables the designer to determine the required external bus width.

In the terminology of claim 1, this disclosure in D1 amounts to determining the maximum latency (in clock periods) allowed for transfer of the block data, determining a minimum number of connections (external bus width as a ratio of the internal bus width) required to transfer the data block with the maximum latency and determining i with i being a value at least the minimum number of required connections.

3.4 The appellant argued that claim 1 is novel over document D1, because D1 does not disclose dividing a data block into smaller groups of bits which each are transferred in a serial fashion by a parallel serial converter, the number of smaller groups corresponding to the number of converters.

The board was not convinced by this argument as it found that in D1 the input data block is divided into smaller groups (i.e. nibbles) of bits that are input in parallel form to respective Cnvt2DblN modules, which transfer the data serially over respective data transfer lines.

The appellant argued further that in D1 the data forming each nibble was spread across all of the transfer lines, whereas according to claim 1 each nibble was transferred over a given one of the transfer lines.

The Board finds however that the term "nibble", in its more general sense, can mean any smaller set of data bits taken from a larger block of data. Hence, in D1, the parts of the data block that are treated by any given Cnvt2DblN module can be considered as being "nibbles" of the input data block in this more general sense.

3.5 Thus, document D1 discloses a method for determining a number of bus connections having all of the features of present claim 1. Claim 1 is therefore considered to lack novelty, Article 54 EPC.

Order

For these reasons it is decided that:

The appeal is dismissed.

The Registrar: The Chairman:

U. Bultmann M. Ruggiu