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Datasheet for the decision of 19 May 2010

Case Number: T 0135/07 - 3.5.02

Application Number: 02789726.3

Publication Number: 1446722

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Language of the proceedings: EN

Title of invention:
User equipment (UE) having a hybrid parallel/serial bus interface

Patentee:
Interdigital Technology Corporation

Opponent:
-

Headword:
-

Relevant legal provisions:
EPC Art. 54

Relevant legal provisions (EPC 1973):

Keyword:
"Novelty - yes (after amendment)"

Decisions cited:
-

Catchword:
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Case Number: T 0135/07 - 3.5.02

D E C I S I O N
of the Technical Board of Appeal 3.5.02
of 19 May 2010

Appellant: INTERDIGITAL TECHNOLOGY CORPORATION
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Decision under appeal: **Decision of the Examining Division of the European Patent Office posted 2 August 2006 refusing European patent application No. 02789726.3 pursuant to Article 97(1) EPC 1973.**

Composition of the Board:

Chairman: M. Ruggiu
Members: G. Flyng
E. Lachacinski

Summary of Facts and Submissions

I. The applicant appealed against the decision of the examining division refusing the European patent application no. 02 789 726.3.

II. The examining division refused the application on the grounds that claims 1 to 9 filed with the letter of 20 June 2006 lacked novelty, Article 54 EPC, in view of the following document:

D1: "Eight Channel, One Clock, One Frame LVDS Transmitter/Receiver", Ed McGettigan, Xilinx Application Note XAPP245 (v1.1), 15 March 2001.

III. In the written statement setting out the grounds of appeal the appellant argued that claim 1 filed with the letter of 20 June 2006 was novel and inventive over document D1.

IV. The board summoned the appellant to attend oral proceedings. In an annex to the summons the board raised questions as to whether certain amendments to the claims were allowable under Article 123(2) EPC and made observations on the novelty of claim 1 filed with the letter of 20 June 2006.

V. Oral proceedings were held before the board on 19 May 2010, during which the appellant submitted an amended set of claims 1 to 9 (main request). The appellant requested that the decision under appeal be set aside and a patent be granted on the basis of claims 1 to 9 of the main request filed during the oral proceedings.

VI. Independent claim 1 filed during the oral proceedings of 19 May 2010 reads as follows:

"1. A hybrid serial/parallel bus interface for use in a synchronous system, the synchronous system having an associated clock, CLK, the bus interface for transferring a data block from a data block demultiplexing device (100) to a data block reconstruction device through i lines comprising:

said data block demultiplexing device (100) having an input configured to receive a data block and demultiplexing the data block into two sets of i nibbles, a set of i odd nibbles and a set of i even nibbles, each nibble having a plurality of bits, wherein even numbered bits of the data block are mapped to the set of i even nibbles and odd numbered bits of the data block are mapped to the set of i odd nibbles;

i even (104) and i odd (102) parallel to serial, P/S, converters, each of a set of i odd nibbles and a set of i even nibbles being sent to a respective set of i P/S converters synchronous with a clock rate of the clock, for converting the received nibbles into serial data;

a first set of i multiplexers (106) for transferring the even i P/S converters (104) set serial data on a positive edge of the clock over i lines and the odd i P/S converters (102) set serial data on a negative edge of the clock over said i lines;

a second set of i demultiplexers (108) for receiving the even and odd transferred serial data and sending the even received serial data to an even buffer (112) and the odd serial data to an odd buffer (110);

i even (116) and i odd (114) serial to parallel, S/P, converters, the i even S/P converters (116) for converting the received even serial data to even parallel data and outputting the even parallel data synchronous with the clock, CLK; and

the i odd S/P converters (114) for converting the odd received serial data to odd parallel data and outputting the odd parallel data synchronous with the clock; and

a data block reconstruction device (112) for combining the even and odd parallel data as said data block."

Claims 2 to 9 are dependent upon claim 1.

VII. The appellant argued essentially that the claims as amended did not introduce fresh subject-matter contrary to Article 123(2) EPC and were novel over document D1, Article 54 EPC.

In particular, whilst document D1 did disclose a set of 8 multiplexers (DDROUT of each OUTSTAGE module) that transferred one set of 8 nibbles from one set of 8 parallel to serial, P/S, converters (RISEPISO of each OUTSTAGE module) on a positive edge of a clock and another set of 8 nibbles from another set of 8 P/S converters (FALLPISO of each OUTSTAGE module) on a negative edge of a clock, the mapping of the bits of the input data block to the nibbles sent to the various P/S converters in document D1 was different to the mapping specified in claim 1.

Specifically, claim 1 required that **even** numbered data bits were mapped to a set of i **even** nibbles, that were

sent to i **even** P/S converters and transferred on **positive** edges of a clock. Similarly, claim 1 required that **odd** numbered data bits were mapped to a set of i **odd** nibbles, that were sent to i **odd** P/S converters and transferred on **negative** edges of the clock. In document D1 however the data transferred on the positive clock edges comprised a mixture of odd and even numbered bits of the input data block. The same was true for the data transferred on the negative clock edges. Thus, the claimed data mapping was novel over document D1.

Reasons for the Decision

1. The appeal is admissible.

2. Amendments, Article 123(2) EPC

Independent claim 1 is based generally on independent claim 23 as filed.

The amendments that have been made compared to claim 23 as filed are derivable from the embodiment of figure 17 and the corresponding description (see WO 03/046737, paragraph [0045]).

In particular, i even and i odd P/S devices are shown in figure 17 and mentioned in paragraph [0045]. There it is disclosed that the data block is "*demultiplexed into two (even and odd) sets of i nibbles*" and that "*each set of the i nibbles is sent to a respective set of i P/S devices 102, 104*". Furthermore, it is stated in paragraph [0045] that "*each buffer 112, 110 receives a corresponding even and odd bit and holds that value*

for a full clock cycle". In the board's view it is directly and unambiguously derivable at least from this statement that the even and odd nibbles are composed respectively from even and odd numbered bits of the input data block. Furthermore, paragraph [0032] of the original description and figure 5 disclose an approach in which the bits of a data block are mapped so as to interleave across two nibbles.

For these reasons the board finds that the amendments according to present claim 1 do not contravene Article 123(2) EPC.

3. Novelty Article 54 EPC

3.1 Document D1 discloses an eight channel, one clock, one frame low-voltage differential signalling transmitter/receiver (see page 1, title and summary). According to the introduction (page 1), the transmitter implements 8 to 1 serialisation, and that is why the DATA input port of the transmitter is 64-bits wide, while the TXN_data / TXP_data differential pair lines are only 8-bits wide. From this disclosure it is clear that the 64 input data bits are transmitted over eight lines, each of which is a differential pair. In the terminology of present claim 1, this corresponds to i = 8 lines.

In table 1 of D1 (see page 2) it is disclosed that data presented at the 64-bit data input bus is transmitted to the receiver in LSW to MSW order. E.g. <7:0>, <15:8>, <23:16>, <31:24>. . . <63:56>. Thus it is disclosed that firstly the bits numbered 0 to 7 of the input data block are transmitted in parallel over the

eight differential lines, then the bits 8 to 15, then the bits 16 to 23 and so on.

Figure 3 of D1 shows a block diagram of the transmitter. It shows the 64-bit-wide input data block (DATA<63:0>) being fed to 8 DDR (double data rate) output stages (OUT_D0 to OUT_D7), which transmit a series of 8-bit data words over the 8-bit-wide differential transmission line (TXP_data<7:0>, TXN_data<7:0>).

The DDR output stages are described in the section "*OUTSTAGE Overview*" from page 4. There it is explained that *the OUTSTAGE block performs as an 8-bit serializer*. Furthermore, it is disclosed that *the 8-bit data from the CLK1X domain is loaded in two 4-bit parallel-to-serial converters. The even bits (6, 4, 2, 0) are transferred during the falling edges of CLK4X and a rising edge of TXP_clk. The odd bits (7, 5, 3, 1) are transferred during the rising edges of CLK4X and a falling edge of TXP_clk*.

Figure 8 of D1 shows a block diagram of the OUTSTAGE module. It shows four data bits referenced *DATA<6,4,2,0>* being fed to a 4-bit P/S converter (*RISEPISO*) and four data bits referenced *DATA<7,5,3,1>* being fed to another 4-bit P/S converter (*FALLPISO*). The two 4-bit serial outputs of the two 4-bit P/S converters are fed to a double data rate flip-flop output (*DDROUT*) module, which is further described in the section *DDROUT Overview* on pages 6 and 7.

Figure 9 of D1 shows the OUTSTAGE waveforms, with data bits numbered 3, 5, 7, 1 being sent when a clock CLK4X

is positive and data bits numbered 4, 6, 0, 2 being sent when the clock CLK4X is negative.

Figure 12 of D1 shows the waveforms of the double data rate flip-flop (*DDRFD*) and the output waveform Q shows again the data bits numbered 1, 3, 5, 7 being sent when CLK4X is positive and the data bits numbered 0, 2, 4, 6 being sent when CLK4X is negative.

Figure 15 of D1 shows a block diagram of the receiver. It shows the 8-bit-wide differential transmission line (RXP_data<7:0>, RXN_data<7:0>) feeding a high speed receiver module (HSRX) which outputs raw data on a 64-bit bus (raw_data<63:0>). The raw data is fed to a FIFO block for queuing (see page 8, "Receiver"). Figure 17 shows a block diagram of the HSRX, with eight octal data rate registers ODR_D0 to ODR_D7). These comprise a tree structure of DDR registers and a snapshot module (SNAP8), see page 12 "ODR_REG Overview" and figure 21.

3.2 The eight RISEPISO converters in the eight OUTSTAGE modules of the D1 device each serialise four data bits. Hence, the board finds that the eight RISEPISO converters can be considered to be a set of i = 8 P/S converters that serialise a set of i = 8 4-bit nibbles in the sense of claim 1 of the present application.

Similarly, the eight FALLPISO converters in the eight OUTSTAGE modules of the D1 device each serialise another four data bits and hence the board considers them to be another set of i = 8 P/S converters that serialise another set of i = 8 4-bit nibbles in the sense of claim 1 of the present application.

Furthermore, the board considers the eight DDROUT modules in the eight OUTSTAGE modules of the D1 device to be a set of i = 8 multiplexers which serially transfer, over a set of i = 8 lines, one set of 4-bit data nibbles from one set of P/S converters on a negative edge of the clock CLK4X and another set of 4-bit data nibbles from another set of P/S converters on a positive edge of the clock CLK4X.

The DDR registers within the eight ODR registers of D1 are serial to parallel (S/P) converters. Within each ODR (see figure 21) it is possible to identify DDR registers (DDR2XF and DDR2XR) that handle the 4 data bits (0, 2, 4, 6 and 1, 3, 5, 7) which correspond to the nibbles of data sent from the corresponding FALLPISO and RISEPISO of the transmitter. These DDR registers can be considered to be two sets of i = 8 S/P converters in the sense of claim 1.

The SNAP8 modules of D1 and the subsequent FIFO module combine the received data to reconstruct the 64-bit data block.

3.3 The question remains whether document D1 discloses the features of claim 1 that specify the mapping of **even** and **odd** numbered bits of the input data block to respective sets of i **even** and i **odd** nibbles that are sent to respective sets, i **even** and i **odd**, of P/S converters and the transferral of the **even** data on a positive edge of a clock and the **odd** data on a negative edge of the clock.

3.3.1 Given that table 1 makes it clear that the bits 0 to 7 comprising the least significant word (LSW) of the input data block are transmitted in parallel, it is evident that the bits of the least significant word must be mapped with one bit to each of the eight OUTSTAGE modules for simultaneous transmission over the eight lines. Indeed, the same must be true for each word of the input data block. Thus, it is evident that the bit numbering 0 to 7 used in the description of the OUTSTAGE module uses a different numbering scheme to the one used for the 64-bit input data block and that the bits 0 to 7 input to any given OUTSTAGE module are not the same as the bits 0 to 7 comprising the least significant word (LSW) of the input data block. Hence the designations "*odd bits*" and "*even bits*" in the section "OUTSTAGE Overview" (page 4) refers to the numbering 0 to 7 of the data bits applied to any given OUTSTAGE module and not necessarily to the numbering 0 to 63 of the bits of the input data block.

3.3.2 Document D1 does not specify exactly how the individual data bits of the input data block are mapped to the OUTSTAGE modules. However given that each of the eight 8-bit words (LSW to MSW) of the input data block must be mapped across all eight OUTSTAGE modules for simultaneous transmission over the eight lines, it is evident that the eight data bits input to any given OUTSTAGE module must comprise one data bit from each of the eight 8-bit words (LSW to MSW) of the input data block.

3.3.3 The appellant has argued that in D1 the bits of the input data block would be mapped onto the eight OUTSTAGE modules (OUT_D0, OUT_D1, etc) as follows:

(note: the following table is based on the bit flow diagram submitted by the appellant in the oral proceedings, but uses the bit numbering 0 to 63 disclosed in D1 rather than the renumbering D1 to D64 used in the appellant's diagram.)

OUT_D0: bits 0, 8, 16, 24, 32, 40, 48, 56;
OUT_D1: bits 1, 9, 17, 25, 33, 41, 49, 57;
OUT_D2: bits 2, 10, 18, 26, 34, 42, 50, 58;
...
...
OUT_D7: bits 7, 15, 23, 31, 39, 47, 55, 63.

3.3.4 Whilst the board does not find a disclosure of this particular mapping in D1, it does consider it to be a most likely mapping given the transmitter/receiver structure disclosed in document D1.

This mapping shows that it is at least possible within the disclosure of D1 that the four even numbered OUTSTAGE modules (OUT_D0, OUT_D2, etc) of the OUTSTAGE modules would receive the even numbered bits of the input data block, whilst the four odd numbered OUTSTAGE modules would receive the odd numbered bits of the input data block. This might allow for the RISEPISOs and the FALLPISOs in the even numbered OUTSTAGE modules to be considered notionally as a set of eight even P/S converters and for the RISEPISOs and the FALLPISOs in the odd numbered OUTSTAGE modules to be considered notionally as a set of eight odd P/S converters in the sense of present claim 1. However, with the RISEPISOs and the FALLPISOs clocked as disclosed in D1, a mixture of even and odd data would be sent on each edge of the

clock, so it would not be the case that the **even** data would be transferred on a **positive** edge of a clock and the **odd** data on a **negative** edge of the clock as set out in claim 1.

3.3.5 Thus, document D1 does not directly and unambiguously disclose the mapping and clocked transferral of even and odd numbered bits of the input data block as specified in present claim 1. For this reason, present claim 1 is to be considered novel with respect to document D1, Article 54 EPC.

4. The features of present claim 1 defining the mapping of the bits of the data block to the odd and even nibbles were not comprised in the claims that formed the basis of the contested decision. Hence, with the addition of these features an entirely new situation has been created that was not considered by the department of first instance.

For this reason the board considers it appropriate to make use of its power under Article 111(1) EPC to remit the case to the department of first instance for further prosecution, in particular for examination of inventive step.

Order

For these reasons it is decided that:

1. The decision under appeal is set aside.

2. The case is remitted to the department of first instance for further prosecution.

The Registrar: The Chairman:

U. Bultmann M. Ruggiu