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# Datasheet for the decision of 28 April 2010

**Case Number:** T 0018/07 - 3.5.02

**Application Number:** 00955071.6

**Publication Number:** 1315286

**IPC:** H03F 1/02

**Language of the proceedings:** EN

**Title of invention:**
Multistage amplifier

**Applicant:**
MITSUBISHI DENKI KABUSHIKI KAISHA

**Opponent:**
-

**Headword:**
-

**Relevant legal provisions:**
EPC Art. 54, 56, 123(2)

**Relevant legal provisions (EPC 1973):**
-

**Keyword:**
"Inventive step - yes (after amendment)"

**Decisions cited:**
T 0119/82

**Catchword:**
-

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Beschwerdekammern | Boards of Appeal | Chambres de recours

**Case Number:** T 0018/07 - 3.5.02

# D E C I S I O N
**of the Technical Board of Appeal 3.5.02**
**of 28 April 2010**

**Appellant**: MITSUBISHI DENKI KABUSHIKI KAISHA
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**Representative**: Pfenning, Meinig & Partner GbR
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**Decision under appeal:** **Decision of the Examining Division of the European Patent Office posted 27 July 2006 refusing European application No. 00955071.6 pursuant to Article 97(1) EPC 1973.**

**Composition of the Board:**

**Chairman:** M. Ruggiu
**Members:** G. Flyng
E. Lachacinski

## Summary of Facts and Submissions

I. The applicant appealed against the decision of the examining division refusing the European patent application No. 00 955 071.6.

II. In the contested decision, the examining division held inter alia that claim 1 on file at that time lacked an inventive step, Article 56 EPC, in view of the following documents:

D1: US 4 532 477
D2: EP 0 451 909 A2.

The examining division also observed that claims 2 and 3 on file at that time were not clear, Article 84 EPC, and lacked an inventive step, Article 56 EPC.

III. Oral proceedings were held before the Board on 28 April 2010. The appellant requested that the decision under appeal be set aside and that a patent be granted in the following version:

Description:

– Pages 1, 3, 3a, 4, 5, 6 and 8 received during the oral proceedings of 28 April 2010;
– Pages 2, 7 and 9 to 12 as originally filed upon entry into the European phase;

Claims:

– Nos. 1 and 2 received during the oral proceedings of 28 April 2010;

Drawings:

– Sheets 1/5 to 5/5 as originally filed upon entry into the European phase.

IV. Claim 1 reads as follows:

"A multistage amplifier having a plurality of cascaded amplifiers (12, 14, 16), each comprising a GaAs FET or HEMT, wherein a bias condition of at least one amplifier (12, 14) among said amplifiers (12, 14, 16) other than a last-stage amplifier (16), said at least one amplifier comprising a GaAs FET or HEMT which is set in consideration of the relation between an idle current and a saturation current,
characterized in that
said bias condition is set such that said idle current is less than a tenth of said saturation current, resulting in a characteristic where the gain first increases and then decreases with respect to the input power and the phase lags with respect to the input power so as to perform distortion compensation on the phase characteristic and on the gain characteristic."

Claim 2 is dependent on claim 1.

V. The appellant argued in essence that the amendments made to the application documents did not offend Article 123(2) EPC, and that the claimed subject-matter was not obvious in view of the cited prior art. In particular, none of the prior art documents disclosed that biasing a GaAs FET or HEMT of an amplifier other than the last stage amplifier such that the idle current was less than a tenth of the saturation current allowed to perform distortion compensation on the phase characteristic and on the gain characteristic.

## Reasons for the Decision

1. The appeal is admissible.

2. *Amendments*

2.1 According to present claim 1, the amplifiers of the multistage amplifier are "cascaded". The term "cascaded" defines the arrangement disclosed in figure 3 of the application more precisely than the term "connected in series to one another" that was used in claim 1 as filed.

The feature of claim 1 that each amplifier comprises a GaAs FET or HEMT is directly and unambiguously derivable from paragraph [0027] of the application as filed (see EP 1 315 286 A1).

The feature of claim 1 that the "bias condition is set such that said idle current is less than a tenth of said saturation current" is directly and unambiguously derivable from claim 2 as originally filed.

It is directly and unambiguously derivable from paragraphs [0031] and [0032] of the application as filed that setting the idle current to be less than a tenth of the saturation current results in a characteristic where the gain first increases and then decreases with respect to the input power and the phase lags with respect to the input power. Furthermore, it is directly and unambiguously derivable from paragraph [0051] of the application as filed that this enables distortion compensation to be performed on the phase characteristic and on the gain characteristic.

2.2 Dependent claim 2 is supported by dependent claim 3 as filed.

2.3 For the above reasons the amendments to the claims are considered not to offend Article 123(2) EPC.

3. *Novelty and Inventive Step*

3.1 Document D1 discloses distortion compensation circuitry 10, comprising cascaded GaAs FET stages 100, 116 and 117, disposed in the input signal path of (i.e. cascaded with) a GaAs FET microwave power amplifier 150 (see column 2, lines 25 to 29 and figure 1). The FET 115 of each stage of the distortion compensation circuitry 10 is biased for class A operation such that the DC component of the drain current is between 10 and 75% of the short-circuit drain current (see column 3, lines 29 to 40).

Thus document 1 discloses a multistage amplifier in accordance with the preamble of present claim 1, i.e. with a plurality of cascaded amplifiers, each comprising a GaAs FET, wherein a bias condition of at least one amplifier other than the last-stage amplifier is set in consideration of the relation between idle current and saturation current.

3.2 According to one of the characterising features of present claim 1, the bias condition is set such that the idle current is less than a tenth of the saturation current. This clearly goes against document D1's teaching to set the biasing to at least 10% of the short-circuit (i.e. saturation) current, a level which

according to D1 assures that gain compression or AM/AM conversion is virtually nonexistent (see column 3, lines 29 to 40). Thus, the subject-matter of claim 1 has to be considered novel over document D1, Article 54 EPC.

3.3 If the skilled person, starting from document D1, were to consider a bias level less than a tenth of the saturation current, it would be apparent to him from the disclosure of D1 that this would no longer assure that gain compression or AM/AM conversion is virtually nonexistent. This would be an apparently disadvantageous modification. According to established practice, a disadvantageous modification is not considered as involving an inventive step if the skilled person could clearly predict the disadvantages, if his assessment was correct and if the predictable disadvantages were not compensated by any unexpected technical advantage (see Case Law of the Boards of Appeal, fifth edition, December 2006, I.D.8.5 and T 119/82, OJ 1984, 217).

3.4 In the present application it is disclosed that by setting the bias level of an amplifier stage to less than a tenth of the saturation current, a gain characteristic is obtained where the gain first increases and then decreases with respect to the input power (see paragraphs [0031] and [0041] and figure 5(b-3)). With this bias condition it is possible, according to paragraph [0051] of the application, to perform distortion compensation not only on the phase characteristic but also on the gain characteristic. With this constitution, according to paragraph [0052], no attenuator or the like is required and a small

distortion compensation circuit can be achieved. These technical advantages are specified in present claim 1.

3.5 The above technical advantages are not suggested in any way by the disclosure of document D1. On the contrary, D1 discloses to use RF attenuators between amplifier stages of the distortion compensation circuit (see column 2, lines 58 to 64).

3.6 Document D2 discloses a predistortion linearizer that comprises essentially a single GaAs FET which carries out the functions both of the gain expander amplifier for recovery of the amplitude distortion of the power amplifier and generator of a command signal for a phase shift element for recovery of the phase distortion of the power amplifier (see column 2, lines 31 to 41).

Whilst it is stated in D2 that the GaAs FET is kept "in under-polarization conditions, i.e. with the working point near the pinch-off region (low values of drain-source current Ids and gate-source voltage Vgs)" (see column 4, lines 5 to 11), there is no indication that by setting the bias condition of the predistortion linearizer's transistor to less than a tenth of the saturation current it is possible to perform distortion compensation on both the phase characteristic as well as the gain characteristic. On the contrary, D2 always uses a phase shift element to provide correction of phase distortion.

3.7 For the above reasons the board concludes that the skilled person, starting from document D1 and considering setting the bias level of an amplifier stage to the apparently disadvantageous level of less

than a tenth of the saturation current, could not have expected for this to enable distortion compensation not only of the phase characteristic but also of the gain characteristic. Such a choice of bias level would therefore provide an advantage that was not expected by the skilled person. For these reasons the subject-matter of present claim 1 is considered to involve an inventive step within the meaning of Article 56 EPC. The same applies to claim 2, as it is dependent on claim 1.

## Order

## For these reasons it is decided that:

1. The decision under appeal is set aside.

2. The case is remitted to the department of first instance with the order to grant a patent in the following version:

Description:

– Pages 1, 3, 3a, 4, 5, 6 and 8 received during the oral proceedings of 28 April 2010;
– Pages 2, 7 and 9 to 12 as originally filed upon entry into the European phase;

Claims:

– Nos. 1 and 2 received during the oral proceedings of 28 April 2010;

Drawings:

– Sheets 1/5 to 5/5 as originally filed upon entry into the European phase.

The Registrar: The Chairman:

U. Bultmann M. Ruggiu