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Datasheet for the decision of 26 November 2009

Case Number: T 1779/06 - 3.5.01

Application Number: 00122104.3

Publication Number: 1098249

IPC: G06F 12/08

Language of the proceedings: EN

Title of invention:
Segmenting cache to provide varying service levels

Applicant:
EMC CORPORATION

Opponent:
-

Headword:
Segmenting cache/EMC

Relevant legal provisions:
EPC Art. 123(2)

Relevant legal provisions (EPC 1973):
EPC Art. 56, 84

Keyword:
"Clarity (no)"
"Added subject-matter (yes)"
"Inventive step (no)"

Decisions cited:
-

Catchword:
-

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Case Number: T 1779/06 - 3.5.01

D E C I S I O N
of the Technical Board of Appeal 3.5.01
of 26 November 2009

Appellant: EMC CORPORATION
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Representative: Patentanwälte
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Decision under appeal: **Decision of the Examining Division of the European Patent Office posted 3 July 2006 refusing European patent application No. 00122104.3 pursuant to Article 97(1) EPC 1973.**

Composition of the Board:

Chairman: S. Steinbrener
Members: S. Wibergh
P. Schmitz

Summary of Facts and Submissions

I. This appeal is against the decision of the examining division to refuse European patent application No. 00122104.3.

II. The following documents will be referred to:

D1: US-A-4 371 929
D5: US-A-5 774 682.

III. The independent claims 1 (filed with letter dated 15 May 2006), 15 and 31 (filed with letter dated 3 February 2003) on which the examining division's decision is based read (omitting the reference signs):

1. A method of storing data in a cache memory of a storage device, wherein said cache memory having a first segment and at least one second segment, said method comprising:
mapping said first segment of the cache memory to each of a first plurality of external host systems coupled to the storage device; and
mapping said at least one second segment of the cache memory to each of at least one second plurality of external host systems coupled to the storage device, said second plurality being different from said first plurality, wherein at least a portion of the second segment of the cache memory is not part of the first segment of the cache memory.

15. A cache memory of a storage device, comprising:
the cache memory;
further characterized by comprising:

a first segment of the cache memory having mapped thereto each of a first plurality of external host systems coupled to the storage device; and
at least one second segment of the cache memory having mapped thereto each of a second plurality of external host systems coupled to the storage device, said second plurality being different from said first plurality, wherein at least a portion of the second segment of the cache memory is not part of the first segment of the cache memory.

31. A computer program product that stores data in a cache memory of a storage device, comprising:
executable code for executing the method according to any one of the preceding Claims 1-14.

IV. According to the decision appealed, the subject matter of claims 1 and 15 did not involve an inventive step over a combination of D1 and D5; claims 3, 15, 17 and 28 were not clear; and claim 31 contained subject-matter extending beyond the content of the application as filed.

V. In the statement setting out the grounds of appeal dated 13 November 2006 the appellant requested that the decision under appeal be set aside. Maintaining the claims on file, it argued as follows:

The method of claim 1 involved an inventive step. According to this method a cache memory of a storage device was subdivided into at least two segments, a first segment and at least one second segment, said first segment was mapped to each of a first plurality of external host systems, and said second segment was

mapped to each of at least one second plurality of external host systems, wherein said first and second pluralities were different from one another, and wherein at least a portion of the second segment was not part of the first segment. Document Dl was considered to be the closest prior art document. Dl disclosed a cache memory partitioned into so-called storage regions, wherein each storage region was uniquely associated with a host adapter. The method of claim 1 was different in that a plurality of hosts was assigned to each of at least two segments of the cache memory. Mapping each host to one individual segment of a cache memory depending on a number of host systems required a relatively large cache memory and was inefficient in terms of temporarily providing a larger cache memory size to individual hosts. The problem to be solved by the present invention was to — depending on a number of host systems — reduce the cache memory size, improving the cache memory performance, and furthermore enabling different levels and types of services to different subsets of hosts. This problem was solved by mapping different pluralities of host systems to different segments of the cache memory. The different segments of such cache memory might offer different cache performance to the pluralities of host systems mapped thereto. Mapping different pluralities of host systems to different cache memory segments was not obvious to the person skilled in the art when considering D1 alone or when considering D1 in combination with D5.

D5 disclosed mapping the entire cache of a cache memory to all of a number of host systems. Taking a number of host systems, Dl disclosed segmenting the cache into a

number of segments corresponding to the number of host systems and mapping each host to an individual segment, while D5 disclosed to map all of these host systems to the (not segmented) cache memory. Even a combination of those prior art documents did not teach the person skilled in the art segmenting the cache memory into a number of segments being smaller than the number of host systems and to map a plurality of host systems to each of those segments. The method of the present invention therefore could not be obtained by the person skilled in the art from Dl and D5. Furthermore, based on the information obtained from Dl the person skilled in the art would not consider mapping more than one host system to one cache memory segment due to the problems described in Dl caused by mapping more than one host to a cache segment.

The grounds did not refer to the examining division's objections under Articles 84 and 123(2) EPC 1973.

VI. In a communication accompanying a summons to oral proceedings which had been requested by the appellant on an auxiliary basis, the Board pointed out that the only difference between the subject-matter of claim 1 and the prior art known from D1 was that a plurality of host systems was assigned to each cache segment. The technical problem might be formulated as finding a way to assign additional hosts to the known storage device. Assigning a host to an existing segment, rather than creating a new one for it, would seem to be an obvious idea at least if, for example, the added host was a back-up device, active only if the regular host failed, or was used at different times of the day. Also the addition of arbitrary hosts may have been obvious. The

appellant's counter-argument that D1 mentioned problems caused by mapping more than one host to a cache segment would only be indicative of an inventive step if the invention overcame such problems. It appeared however that in particular the "bottle-neck" problem mentioned in paragraph [0005] of the present patent application (as published) would hamper the invention to some degree. Merely accepting expected disadvantages was not inventive.

Furthermore, the examining division's objection under Article 84 EPC 1973 against claim 15 that the claimed cache memory comprised itself, appeared justified.

Finally, Article 123(2) EPC appeared to be infringed. Claim 31, added at the examination stage, was understood as being directed to a computer program for storing data in a cache memory by performing the method steps of any one of claims 1-14. The appellant had admitted that the application as originally filed did not explicitly disclose such a program but had argued that it was obvious that methods of storing data in a cache memory were implemented as software. Claim 1, although directed to a method of storing data, was however mainly concerned with the mapping of cache segments to different host systems. The Board doubted if the original application disclosed that these mapping steps were performed by software. Paragraph [0041] of the description might in fact suggest that they were not: "The particular allocations among groups may be made for a variety of reasons, such as group 1 having more external host systems or having external host systems that have greater storage needs".

VII. By letter dated 19 October 2009 the appellant withdrew its request for oral proceedings and requested a decision according to the state of the file. Accordingly, the oral proceedings were cancelled.

Reasons for the Decision

The Board maintains the objections, based on Articles 56 and 84 EPC 1973 and Article 123(2) EPC, raised in its communication (see point VI above). Thus, the appeal must be dismissed.

Order

For these reasons it is decided that:

The appeal is dismissed.

The Registrar: The Chairman:

T. Buschek S. Steinbrener