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**Datasheet for the decision
of 3 March 2009**

Case Number: T 1646/06 - 3.4.03

Application Number: 99106561.6

Publication Number: 0948031

IPC: H01L 21/00

Language of the proceedings: EN

Title of invention:

Semiconductor fabrication line with contamination preventing function

Applicant:

NEC Electronics Corporation

Opponent:

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Headword:

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Relevant legal provisions:

-

Relevant legal provisions (EPC 1973):

EPC Art. 54, 56

Keyword:

"Main request and first auxiliary request: Novelty (no)"

"Second auxiliary request: inventive step (no)"

Decisions cited:

-

Catchword:

-



Case Number: T 1646/06 - 3.4.03

D E C I S I O N
of the Technical Board of Appeal 3.4.03
of 3 March 2009

Appellant: NEC Electronic Corporation
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Decision under appeal: Decision of the Examining Division of the
European Patent Office posted 9 June 2006
refusing European application No. 99106561.6
pursuant to Article 97(1) EPC.

Composition of the Board:

Chairman: G. Eliasson
Members: V. L. P. Frank
T. Bokor

Summary of Facts and Submissions

- I. This is an appeal from the refusal of application 99 106 561 for lack of novelty (Article 54 EPC 1973).
- II. At oral proceedings before the board, the appellant applicant requested that the decision under appeal be set aside and that a patent be granted on the basis of claim 1 filed as main request with letter dated 3 February 2009, or in the alternative on the basis of claim 1 of the 1st or 2nd auxiliary requests, also filed with letter dated 3 February 2009.
- III. Claim 1 of the main request reads (the amendments with respect to the version refused by the examining division have been marked by the board):

"A semiconductor fabrication line with contamination preventing function, comprising:
a mainstream line (1) suitable for fabricating a semiconductor device from a wafer (5), **where a surface of said wafer is not exposed to the contamination causing material;**
an isolation line (3) separated from said main streamline;
characterized by that said isolation line contains the contamination-including semiconductor fabrication equipments (7-9) of the semiconductor fabrication line **for processing a contamination causing material to said wafer**, such that the contamination causing material for contaminating said mainstream line and appearing on a surface of said wafer is removed from the surface of said wafer in said isolation line after processing, and

after said contamination causing material is removed, said wafer is returned to said main stream line, and said isolation line (3) includes a cleaning equipment for removing said contamination causing material."

Claim 1 of the 1st auxiliary request differs from claim 1 of the main request in that it is further specified at the start of the characterizing portion of the claim that the fabrication line is:

"characterized by that said mainstream line (1) is kept in a low contamination state compared with said isolation line (3),"

Claim 1 of the 2nd auxiliary request differs from claim 1 of the main request in that the following features are added at the end of the claim:

"said main stream line (1) comprises a main stream-line cassette (4a) to load said wafer and said isolation line (3) comprises an isolation-line cassette (4b) to load said wafer; and a wafer transferring mechanism transfers said wafer between said mainstream-line cassette (4a) and said isolation-line cassette (4b)."

IV. The following documents are mentioned in this decision:

D1: Pat. Abs. of Jap., vol. 013, no. 344 & JP 01
102842 A

D2: US 5 404 894 A

D3: Pat. Abs. of Jap., vol. 1997, no. 08 & JP 09
107015 A

V. The appellant applicant argued essentially as follows:

- The inventive concept of the present application consisted in maintaining the mainstream line of a semiconductor fabrication line free from contaminants by creating an isolation line separated from the mainstream line and locating all the contamination-including semiconductor fabrication equipments in the isolation line.
- Documents D1 and D3 related to preventing contaminants from entering a clean vacuum environment and did not disclose an isolation and a mainstream line in the sense of the application.
- Document D2, on the other hand, disclosed a washing station in which wafers were treated with hydrofluoric acid (HF). D2 did not disclose cleaning equipment for removing a contamination causing material. It moreover disclosed processes (ion implantation or ashing) which might be performed in the processing chambers. However these processes also involved contaminating materials. Therefore D2 failed to disclose that all the contamination-including semiconductor fabrication equipments were contained in the isolation line.

Reasons for the Decision

1. The appeal is admissible.
2. *Main and 1st auxiliary request - Novelty*
 - 2.1 Claim 1 of the 1st auxiliary request (AR1) differs from claim 1 of the main request (MR) by the feature that the *"mainstream line (1) is kept in a low contamination state compared with said isolation line"*. A finding of lack of novelty on claim 1 of AR1 forcefully applies also to claim 1 of MR, since the latter comprises all the subject-matter of the former. Therefore, in the following claim 1 of AR1 will be discussed.

- 2.2 Document D2 discloses in the wording of claim 1 of AR1 (reference signs according to this document and explanatory comments were inserted by the board):

A semiconductor fabrication line with contamination preventing function, comprising:

a mainstream line (1st and 2nd conveyor access portions 20 and 70, 1st and 2nd mounting chambers 1 and 6, intermediate transfer chamber 50, 1st and 2nd thermal processing portions 3A and 3B; Fig 1 and column 5, lines 20 to 43) suitable for fabricating a semiconductor device from a wafer, where a surface of said wafer is not exposed to the contamination causing material (in the present case the HF acid used in the washing portion 72);

an isolation line (washing portion 72; column 5, lines 40 to 43) separated from said main streamline; wherein said mainstream line is kept in a low contamination state compared with said isolation line

(as it will be discussed, it is implicit that the HF acid is cleaned from the wafer, so as to not contaminate the remaining portions of the device of D2), said isolation line contains the contamination-including semiconductor fabrication equipments (the HF washing equipment) of the semiconductor fabrication line for processing a contamination causing material to said wafer, such that the contamination causing material for contaminating said mainstream line and appearing on a surface of said wafer is removed from the surface of said wafer in said isolation line after processing, and after said contamination causing material is removed, said wafer is returned to said main stream line, and said isolation line (72) includes a cleaning equipment for removing said contamination causing material (as already mentioned this issue will be addressed below).

- 2.3 The appellant applicant argued that document D2 did not disclose a semiconductor fabrication line with a contamination preventing function. The issue addressed by D2 was instead to keep track of the orientation of the wafer's flat while it was transferred between the different processing chambers (column 2, lines 5 to 13).

In the board's view, the above considerations might be relevant when assessing inventive step, eg whether the skilled person would have considered the device disclosed in D2 as a promising starting point. However, when assessing novelty what has to be considered is what has been made available to the public (Article 54(2) EPC 1973). This requires that for a device claim the features of the devices of the state

of the art be compared with the features of the claimed device.

- 2.4 The appellant applicant further remarked that D2 did not disclose any cleaning equipment or any details on the HF acid washing portion 72. Accordingly, it could not be said that D2 disclosed the cleaning equipment explicitly specified in claim 1 as being a constitutive part of the isolation line.

The board considers, however, that for a person skilled in the field of semiconductor device fabrication it is implicit that a step of silicon dioxide removal by HF acid must be followed by an adequate cleaning step, eg by washing the wafer with high purity water or by blowing it with a nitrogen jet. Silicon wafers grow nearly instantly a thin layer of silicon dioxide when exposed to an oxygen containing atmosphere. It is therefore current practice to remove the oxide layer with HF acid in vacuum or under an inert atmosphere before further processing the silicon wafer. As the HF molecule is very mobile and highly reactive it is imperative to remove it from the wafer so as to prevent it from contaminating the rest of the semiconductor processing equipment.

The board finds, for these reasons, that a cleaning equipment as specified in claim 1 is implicitly disclosed in document D2 as constitutive part of the washing portion 72.

- 2.5 The appellant applicant argued that the gist of the present invention was to locate **all** the contamination-including semiconductor fabrication equipment in the

isolation line (application as filed page 9, lines 7 to 27, page 16, lines 19 to 21; Figure 6). In contrast thereto D2 mentioned ion implantation or ashing as possible processes which might be carried out in the processing chambers 3A and 3B (column 9, lines 60 to 65). These processes, however, involved contaminants, and therefore D2 did not disclose that **all** the contaminating equipment was included in the isolation line. The representative also signaled willingness to amend the claims in order to clarify this aspect.

The board is, however, not persuaded that the application as filed discloses directly and unambiguously that **all** the contamination-including semiconductor fabrication equipment is located in the isolation line and, consequently, such a construction of claim 1 does not have a basis in the application as filed. Therefore, an amendment to claim 1 to specify such restriction would not be permissible under Article 123(2) EPC. Figure 6 and page 9, lines 10 to 12 of the application disclose that "multiple individual lines using the contamination causing materials are provided in the isolation line". This, however, does not imply that **all** the contaminating equipment is so located, but merely that several contaminating equipments can be grouped into a single isolation line, not excluding the presence of contaminating equipment outside the isolation line or in further isolation lines.

- 2.6 In the judgement of the board, the semiconductor fabrication line of claim 1 of the main request and of the 1st auxiliary request is therefore not novel over document D2.

3. *2nd auxiliary request - Inventive step*

3.1 The fabrication line of claim 1 of this request differs from the subject-matter of claim 1 of the MR in that the mainstream line comprises a mainstream line cassette and the isolation line comprises an isolation line cassette and in that a wafer transferring mechanism transfers the wafers between said mainstream line cassette and said isolation line cassette.

3.2 Document D2 discloses wafer cassettes 71 in the wafer cassette chambers 7A and 7B (column 7, lines 21 to 26; Figure 1). A wafer transferring mechanism 61 is provided in the 2nd mounting chamber 6 for transferring the wafers between the cassette chambers (ie the mainstream line) and the washing station 72 (ie the isolation line) (column 7, lines 49 to 55). Exemplarily, the wafer transferring mechanism comprises five conveyor arms 61B while the wafer cassette stores 25 wafers (column 5, lines 44 to 51; column 7, lines 13 to 20 and lines 31 to 35; Figure 3). Consequently, five operations of the conveyor arm are required for transferring the wafers between the mainstream line cassette and the isolation line.

3.3 Document D2, however, does not disclose the use of an isolation line cassette (ie in the washing station 72). It follows that the fabrication line of claim 1 differs from the one disclosed in D2 in the provision of an isolation line cassette.

The problem addressed by this feature can be seen in a more efficient handling of the wafers in the isolation line.

3.4 The use of a cassette in the isolation line is however obvious to the skilled person, since it groups the wafers into a single device and therefore simplifies the HF acid washing and cleaning steps in the isolation line by allowing them to be done on all the wafers in the cassette simultaneously. As document D1 already discloses a transferring mechanism between two different sets of cassettes ("especially devoted cassettes" 5a and "transport cassettes" 2a) the skilled person would have been prompted to introduce isolation line cassettes in the fabrication line of document D2 as well.

3.5 The board concludes therefore that the fabrication line of claim 1 of the 2nd auxiliary request does not involve an inventive step within the meaning of Article 56 EPC 1973.

Order

For these reasons it is decided that:

The appeal is dismissed.

Registrar

Chair

S. Sánchez Chiquero

G. Eliasson