Internal distribution code:
(A) [ ] Publication in OJ
(B) [ ] To Chairmen and Members
(C) [ ] To Chairmen
(D) [X] No distribution

Datasheet for the decision
of 20 October 2009

Case Number: T 1608/06 - 3.5.04

Application Number: 03713171.1

Publication Number: 1497973

IPC: H04N 5/335

Language of the proceedings: EN

Title of invention:
Imaging device and timing generator

Applicant:
Axis AB

Headword:
-

Relevant legal provisions:
-

Relevant legal provisions (EPC 1973):
EPC Art. 56

Keyword:
"Inventive step - (yes) after amendment"

Decisions cited:
-

Catchword:
-

Case Number: T 1608/06 - 3.5.04

D E C I S I O N
of the Technical Board of Appeal 3.5.04
of 20 October 2009

Appellant: Axis AB
                        Emdalavägen 14
                        S-223 69 Lund   (SE)

Representative: Johansson, Magnus
                        Awapatent AB
                        Box 1066
                        S-251 10 Helsingborg   (SE)

Decision under appeal: **Decision of the Examining Division of the**
                               European Patent Office posted 16 May 2006
                               refusing European patent application
                               No. 03713171.1 pursuant to
                               Article 97(1) EPC 1973.

Composition of the Board:

Chairman: F. Edlinger
Members: C. Kunzelmann
                   B. Müller

C2109.D

Summary of Facts and Submissions

I.   The appeal is against the decision of the examining
        division to refuse European patent application
        No. 03 713 171.1, published as WO 03/088653 A1.

II.   The examining division refused the present application
        on the ground that the subject-matter of the claims
        then on file lacked an inventive step. The decision
        under appeal referred to the following documents:

        D1: US 5 581 303 A,
        D4: JP 2001 238138 A and
        D5: US 2002/0135690 A1.

III.   The applicant appealed and filed new claims with the
        statement of grounds of appeal.

IV.   In a communication dated 22 April 2009 under Rule 100(2)
        EPC the board indicated its provisional opinion that
        grant of a patent could only be envisaged once minor
        amendments had been made to the application.

V.   With a letter dated 8 May 2009, in reply to the board's
        communication, the appellant filed claims 1 to 8
        replacing the claims filed with the statement of
        grounds of appeal and replacement pages 2, 2a, 2b, 2c,
        3 and 6 of the description.

VI.   Claim 1 reads as follows.

        "A timing generator (12) for an imaging system,
        comprising:

an output timing signal controller (236; 318), which
output timing signal controller (236; 318) is arranged
to provide a plurality of output signals *at a plurality
of signal lines thereof (414),*
an horizontal position counter and a vertical position
counter (204) arranged to count clock cycles for
keeping track of an x and y coordinate of a pixel
presently handled,
said timing generator (12) being characterized by:
a programmable program memory (220; 316) that is
arranged to comprise program instructions for
controlling the generation of timing signals,
a timing generator controller (222) for processing the
program instructions from the program memory (220; 316),
the timing generator controller (222) including a
decoder (224; 302) for decoding program instructions
from the memory (220; 316), *the decoder (224; 302)
being arranged to output at least one control signal
(402) and a plurality of parallel signals forming a bit
pattern and constituting an output timing signal
specification (404), the output timing signal
specification (404) determining the appearance of the
output signals in response to the decoding of said
instructions,*
*the output timing signal controller (236; 318) being
connected to the timing generator controller (222) for
reception of the at least one control signal (402) and
the output timing signal specification (404), and*
*the output timing signal controller (236; 318) further
comprising means for performing an XOR operation (412)
and comprising at least one selector (406), said means
for performing an XOR operation (412) being arranged to
receive said plurality of output signals (414), to
receive said output timing signal specification (404)*

or a bit pattern of zeros from the selector (406)
depending on the at least one control signal (402), and
to output signals resulting from the XOR operation
between the signals (418) from the selector (406) and
said plurality of output signals (414), wherein the
output from the means for performing an XOR operation
(412) is connected to the plurality of signal lines
(414) of the output timing signal controller (236;
318)."

The amendments in claim 1 with respect to claim 1 on
which the decision under appeal was based have been
indicated in *italics*.

VII.   The reasoning in the decision under appeal can be
        summarised as follows.

        The closest prior art was D4. D5 was used as a
        translation of D4, as D4 was the priority document of
        D5.

        The subject-matter of claim 1 differed from the
        teaching of D4 in that the timing generator was
        programmable like a general purpose microprocessor.
        Therefore the problem to be solved was how to increase
        the flexibility of the timing generator. This problem
        was formulated in D1, column 1, lines 32 to 35. Thus a
        person skilled in the art would have combined the
        teachings of D4 and D1. D1 disclosed a programmable
        program memory that was arranged to comprise program
        instructions for controlling the generation of timing
        signals. D1 also disclosed a timing generator
        controller and an output timing signal controller as
        specified in claim 1 then on file. Therefore a person

skilled in the art would have arrived at the subject-
matter of claim 1 then on file without an inventive
step by combining the teachings of D4 and D1.

VIII. The appellant's arguments can be summarised as follows.

D4 was the closest prior art. The problem of increasing
the flexibility of the timing generator for an imaging
system was already solved in D4 by arranging a computer
that stored edge data and time series data which could
be downloaded to an edge data RAM and a time-series
data RAM. D4 disclosed that this configuration could be
used to change the timing to drive the solid state
imaging device even after the timing generator was
completed. A person skilled in the art would not have
tried to find a solution to the above problem in D1
because D1 concerned the timing of a video display. The
timing of an imaging system was much more complex than
the timing of a video display.

By means of the timing generator according to claim 1
it was possible to add an instruction in the
programmable program memory to provide for altering at
least one of the output signals. The instruction could
be programmed without the programmer knowing the
present state of the other output signals and without
affecting these other output signals. This was possible
by means of an arrangement of a selector and a means
for performing an XOR operation as specified in claim 1.
That is, each output signal line connected to an XOR
operation provided with, for instance, a logical "1"
from the instruction was altered from its present state,
whereas each output signal line connected to an XOR

operation provided with, for instance, a logical "0"
kept its present state.

The objective problem was to facilitate the control of
individual output signals, and D4 did not recognise
this objective problem. In D4 the output signals were
generated as logical combinations of signals from a
time-series data ROM and two edge data ROMs in a mixer.
Thus, according to D4, it was necessary to obtain
information from all the ROMs, of the state of the rest
of the output signals and of the logical function in
the mixer in order to be sure that the alteration did
not alter output signals that should not be affected.
D1 did not provide any teaching that led a person
skilled in the art to the solution of the objective
problem either. Even if a person skilled in the art
tried to combine the teachings of D1 and D4, the
combination failed to disclose all the features of
present claim 1.

IX.   The appellant requested that the decision be set aside
        and a patent be granted based on the new claims. The
        appellant also requested oral proceedings if the
        request was not allowed.

Reasons for the Decision

1.   The appeal is admissible.

2.   *Allowability of the amendments (Article 123(2) EPC)*

2.1   Claim 1 is based on original claim 1 and comprises
        additional features disclosed in the description as

C2109.D

originally filed. Namely the horizontal and vertical
position counters are disclosed in figure 2 and on
page 9, lines 15 to 20, and page 10, lines 26 to 29.
The features specifying the timing generator controller
are disclosed in figure 3 and on page 13, lines 32
to 37, and page 15, lines 3 to 6. The features of the
output timing signal specification are disclosed on
page 19, lines 25 to 35, in conjunction with page 18,
line 36, to page 19, line 4. The features specifying
the output timing signal controller are disclosed in
figures 3 and 4 and on page 20, lines 5 to 30. In
particular the feature of "at least one selector" is
disclosed because the mask selector (406) and the
signal selector (408) in figure 4 relate to distinct
functionalities which are individually disclosed.

2.2   Claims 2 to 6 are original dependent claims 2 to 6.
        Claims 7 and 8 are disclosed in original claims 7
        and 11.

2.3   The description has been amended to acknowledge the
        prior art documents D1 and D4 and has been brought into
        conformity with the current claims.

2.4   Thus the present application documents comply with
        Article 123(2) EPC.

3.   *Inventive step (Article 56 EPC 1973)*

3.1   It is undisputed that none of the available documents
        destroys the novelty of the timing generator according
        to claim 1. The board agrees. Furthermore the appellant
        has not challenged the use of D5 as a translation of
        the closest prior art D4. Hence the board, based on the

presumption that the disclosure of the Japanese patent
application D4, from which the post-published US patent
application D5 derives its priority, is fairly
reflected by D5, will refer to the disclosure of D4 in
the light of D5.

3.2   D4 discloses a timing generator having the features of
        the precharacterising portion of claim 1. More
        specifically, D4 discloses in its embodiment of
        figure 3 a timing generator (14) for an imaging system,
        namely a solid state imaging device such as a CCD
        (see D5, paragraph [0020]). The timing generator (14)
        of D4 comprises an output timing signal controller
        ("combinatorial logic circuit (MIX) block" 60, see D5,
        paragraph [0023]) arranged to provide a plurality of
        output signals at a plurality of signal lines thereof
        (H1, H2, V1 to V4, CH1, CH2, PROC), a horizontal
        position counter (41) and a vertical position counter
        (31) being arranged to count clock cycles to keep track
        of an x and y coordinate of a pixel presently being
        handled (see D5, paragraph [0023]).

3.3   The timing generator disclosed in D4 has some
        flexibility on a general level as to how the timing
        pulses are generated. Repetitive pulse patterns are
        stored as time-series data for several types of timing
        pulses that change in mutually correlated manners. For
        timing pulses that should be set on an individual basis
        the addresses of the leading and trailing edges thereof
        are stored as edge data (see D5, paragraph [0009]).
        Specifically a "time-series data ROM 50 is a memory for
        storing data representing the logical level repetitive
        pattern of an output pulse train." And "edge data
        ROMs 33 and 43 are memories for storing data

representing at what counts of the V-and H-counters 31 and 41 control pulses should change their logical levels" (see D5, paragraph [00023]). Hence by changing the ROMs other timing signals may be produced. In other embodiments an external ROM 70 stores second, alternative time-series data and second, alternative edge data (see figure 8 and D5, paragraphs [0030] and [0031]). A PC 100 may be provided in addition to, or instead of, the external ROM 70 to store third edge data and third time-series data in respective RAMs as a further alternative. With PC 100 the timing pulses can be changed without redesigning the timing generator (see figure 9 and D5, paragraphs [0033] to [0035]).

3.4   The features specified in the characterising portion of present claim 1 (in particular the selector in combination with the XOR means controlled by the timing generator controller processing the instructions from the programmable program memory) have the technical effect of allowing a subset of output signals to be altered without considering any other output signals (see page 20, lines 27 to 30, of the application, instructions "inv_sig <mask>" and "inv_extra <mask>" in Tables 1 and 2). For instance, the output signals may represent an instruction word which is provided as data to several devices which receive timing signals from the timing generator, and certain bits are enable bits which possibly need to be manipulated individually (see page 14, line 15, to page 15, line 2). The board thus concurs with the appellant that the objective technical problem may be seen in facilitating the control of individual output signals.

3.5   D4 does not address the problem of selectively
       manipulating individual bits of the output signal. D1,
       the second document used in the decision under appeal,
       is not concerned with the manipulation of individual
       bits in the output signal either. D1 discloses a timing
       circuit for an object completely different from a CCD,
       namely for a video monitor. The timing circuit has some
       flexibility because it comprises an instruction SRAM.

3.6   A person skilled in the art, familiar with the teaching
       of D4 and faced with the problem of altering a subset
       of output signals individually without considering any
       other output signals, would not have considered
       combining document D1 with the teaching of D4. Firstly,
       D1 concerns a technical field (timing of video displays)
       different from that of D4 (timing of imaging devices
       such as CCDs, which require more complex timing
       signals). Secondly, the particular problem of altering
       a subset of output signals individually without
       considering any other output signals is not discussed
       in D1 and D1 does not disclose any solution to this
       problem. And thirdly, D4 essentially teaches altering
       the output signals by providing alternatives to the
       data stored on the ROMs or, possibly, by downloading
       from a PC a complete set of data into RAMs. But the
       particular solution to the problem, as specified in
       claim 1, is not suggested in D1 or D4. Thus a person
       skilled in the art would not have arrived at the
       subject-matter of present claim 1 by combining
       documents D4 and D1 in an obvious manner.

3.7   The other documents on file are not closer to the
       invention than documents D4 or D1.

3.8   Hence the board judges that the timing generator
        according to claim 1 involves an inventive step
        (Article 56 EPC 1973).

4.   Claims 2 to 8 are dependent on claim 1. Hence their
        subject-matter also involves an inventive step.

5.   Thus the board allows the appeal. Hence there is no
        need to hold oral proceedings.

Order

For these reasons it is decided that:

1.   The decision under appeal is set aside.

2.   The case is remitted to the first instance with the
        order to grant a patent in the following version:
        Description:
        Pages 1, 4, 5 and 7 to 22 as published.
        Pages 2, 2a, 2b, 2c, 3 and 6 filed with the letter of
        8 May 2009.
        Claims:
        No. 1 to 8 filed with the letter of 8 May 2009.
        Drawings:
        Sheets 1/3 to 3/3 as published.

The Registrar: The Chairman:

L. Fernández Gómez   F. Edlinger

C2109.D