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**Datasheet for the decision
of 21 November 2008**

Case Number: T 1561/06 - 3.4.03

Application Number: 99201867.1

Publication Number: 0984670

IPC: H05B 41/29

Language of the proceedings: EN

Title of invention:

High intensity discharge lamp ballast

Applicant:

Simsoarica Ltd.

Opponent:

-

Headword:

High intensity discharge lamp ballast/SIMSOARICA LTD

Relevant legal provisions:

EPC Art. 123(2), 56

Relevant legal provisions (EPC 1973):

-

Keyword:

"Amendments (allowable)"

"Inventive step (yes)"

Decisions cited:

-

Catchword:

-



Case Number: T 1561/06 - 3.4.03

D E C I S I O N
of the Technical Board of Appeal 3.4.03
of 21 November 2008

Appellant: Simsoarica Ltd.
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Decision under appeal: Decision of the Examining Division of the
European Patent Office posted 18 May 2006
refusing European application No. 99201867.1
pursuant to Article 97(1) EPC.

Composition of the Board:

Chairman: V. L. P. Frank
Members: E. Wolff
J. Van Moer

Summary of Facts and Submissions

- I. This is an appeal against the refusal of application 99 201 867 for contravening the provisions of Article 123(2) EPC.
- II. On appeal, the applicant requested grant of a patent on the basis of the request submitted during the oral proceedings.

Independent claim 1 of the request reads as follows:

"1. A high intensity discharge lamp ballast circuit comprising:

a high intensity discharge lamp (19) connected between a first lamp terminal (B) and a second lamp terminal;

first and second MOSFETs (9,10) connected in series between a positive rail (+HT) of a source of high voltage and a negative rail (0V) of the source of high voltage, a node (A) being located at the junction between the first and second MOSFETs (9,10);

a first diode (70) connected in series with the first MOSFET (9) between the positive rail (+HT) and the node (A);

a second diode (71) connected in series with the second MOSFET (10) between the node (A) and the negative rail (0V);

a first fast recovery diode (15) connected between the node (A) and the positive rail (+HT), in antiparallel with the first MOSFET (9) and the first diode (70);

a second fast recovery diode (16) connected between the node (A) and the negative rail (0V), in

antiparallel with the second MOSFET (10) and the second diode (71);

a resonant circuit comprising a capacitor (18) connected in parallel with the lamp (19) and an inductor (17) connected in series between the first lamp terminal (B) and the node (A), whereby the first MOSFET (9) is operable to connect the resonant circuit (17,18) to the positive rail (+HT) and the second MOSFETs (10) is operable to connect the resonant circuit (17,18) to the negative rail (0V);

control means (6) for alternately operating the first and second MOSFETs (9,10) to supply current to the resonant circuit (17,18), the alternation occurring in a first mode at a first switching frequency that causes the resonant circuit (17,18) to resonate and in a second mode at a second switching frequency that does not cause the resonant circuit (17,18) to resonate; and

current limiting means (5,20) for limiting the electrical current through the lamp (19);

CHARACTERIZED IN THAT

each of the first and second diodes (70, 71) is capable of blocking a reverse voltage substantially equal to the voltage between the positive rail (+HT) and the negative rail (0V)."

The remaining claims 2 to 12 of the request are dependent claims.

III. Claim 1 as originally filed reads as follows:

"1. A high intensity discharge lamp ballast circuit comprising:

a high intensity discharge lamp (19) connected between a first lamp terminal (B) and a second lamp terminal;

a resonant circuit (17,18), to which the first lamp terminal (B) is connected;

first switching means (9) operable to connect the resonant circuit (17,18) to a positive rail (+HT) of a source of high voltage;

second switching means (10) operable to connect the resonant circuit (17,18) to a negative rail (OV) of the source of high voltage;

control means (6) for alternately operating the first and second switching means (9,10) to supply current to the resonant circuit (17,18), the alternation occurring in a first mode at a first switching frequency that causes the resonant circuit (17,18) to resonate and in a second mode at a second switching frequency that does not cause the resonant circuit (17,18) to resonate; and

current limiting means (5,20) for limiting the electrical current through the lamp (19)."

IV. The following documents are cited in this decision

D3 = EP-0 408 121 A

D4 = US-4 926302 A

V. The appellant's arguments can be summarized as follows.

The invention concerned power control circuits for high intensity discharge lamps

Document D3 addressed the need to protect the circuit against DV/DT failures of the parasitic diodes of the MOSFETs. Schottky diodes connected in series with the switching transistors solved that problem.

The invention concerned a different problem, which arose from currents flowing on account of the parasitic body capacitance of the MOSFETs. These currents lead to unacceptably high losses. In order to reduce these losses, the diodes connected in series with the MOSFETs had to be able to withstand substantially the full reverse voltage (approximately 400V in the example of Figure 5) applied to whichever MOSFET was turned off. Schottky diodes as used in document D3 not only had relatively long recovery times but at the time the application was filed were unsuitable for high reverse voltages and even now were still unsuitable for reverse voltages greater than about 150V to 200V.

Reasons for the Decision

1. The appeal is admissible.
2. *Amendments*
 - 2.1 Claim 1 of the request differs from claim 1 as originally filed by including specific details of the resonant circuit and of the switching means.
 - 2.2 The circuit of Figure 5 uses MOSFETs 9 and 10 connected serially with diodes 70 and 71 respectively. MOSFET 9 and diode 70 are connected between the positive rail and node A, while MOSFET 10 and diode 71 are connected

between node A and the 0V rail. The polarity of the diodes 70 and 71 is arranged such that when the MOSFET serially connected to the diode is in the ON condition the diode can conduct current in the same direction as the MOSFET. The diodes 70, 71 act to block the flow of current in the body diodes of the MOSFETs 9, 10. Further, the diodes 70,71 also act to block the flow of capacitive currents associated with the drain-to-source capacitance of the inactive MOSFET that would otherwise be commutated by the active (switching) MOSFET during the second of the two discrete modes of operation (original application, page 12, lines 24 to 29).

- 2.3 When the circuit in Fig. 5 operates in its second mode of operation, that is, after the lamp has been struck, the frequency control circuit sets the associated oscillator 1 to switch at a relatively low frequency, typically of the order of tens or hundreds of Hz (column 6, lines 31 to 35) as compared to a typical frequency of several tens kHz during operation at resonance in the first mode (column 5, lines 10-12). The output signal of the oscillator 1 is applied to one of the inputs of AND-gate 3 and the inverse output is applied to one of the inputs of AND-gate 4. The second input to each AND-gate is the output of the current limiter 5. As long as the current in the ballast circuit as sensed via transformer winding 28 does not exceed a set value, the output from the current limiter to both AND-gates is ON. Accordingly, under these conditions, the frequency control circuit and its associated oscillator 1 alone control the operation of the MOSFETs 9 and 10. On account of the inverse input to AND-gate 4, either MOSFET 9 conducts and MOSFET 10 is off, or MOSFET 10 conducts and MOSFET 9 is off. This

provides a low frequency square wave current to the lamp. Superimposed on this low frequency square wave is the output of the current limiting circuit 5 which maintains the current to the lamp between two threshold levels by switching the "active" MOSFET on and off at high frequency, which results in a high frequency ripple being superimposed on the low frequency square wave, as shown in Fig. 3 (page 9, line 16 to page 10, line 14; page 11, lines 1-13). More particularly for the duration of one half cycle of the square wave, MOSFET 10 remains off and MOSFET 9 is being alternately switched on and off at high frequency so that node A is being alternately connected to and disconnected from the high voltage rail HT.

2.3.1 When MOSFET 9 connects node A to the HT rail, the voltage at node A will be close to +HT (e.g. 400V). When MOSFET 9 disconnects node A from the HT rail, inductor 17 causes reactive current to continue to circulate through the lamp 19, the 0V rail, diode 16 and node A. Therefore the voltage at node A will be close to 0V (differing merely by the small forward voltage drop across diode 16). Hence, the voltage at node A is oscillating at high frequency between approximately 0V and +HT (page 10, lines 16-30).

2.3.2 Owing to the inherent and parasitic drain-to-source capacitance of MOSFET 10 between the upper and lower terminals as shown in Fig. 5, the drain (upper terminal) of MOSFET 10 would, in the absence of diode 71, be directly connected to node A while the source (lower terminal) of MOSFET 10 is directly connected to the 0V rail. It follows that the voltage across the MOSFET would oscillate in the same way as the voltage at node

A and the drain-to-source capacitance of the MOSFET would charge and discharge at high frequency. Because a capacitor, and hence the drain-to-source capacitance, has low impedance at high frequency, the charging currents would be high and cause significant losses in the active MOSFET.

2.3.3 The diode 71 prevents these losses by first allowing the parasitic body capacitor of MOSFET 10 to charge when the voltage at node A first rises to + HT, but then blocking the reverse current that would allow the capacitor to discharge when the voltage at node A falls close to 0V (page 12, lines 25-29). Thus the voltage at the drain of the MOSFET remains close to +HT and hence a reverse voltage is applied across the diode 71 close to the voltage applied between the +HT voltage rail and the 0V voltage rail.

2.4 The further details of the resonant circuit which have been added to claim 1 reflect the content of the description relating to Figure 5.

2.5 The board is therefore satisfied that the ballast circuit of claim 1 is directly and unambiguously derivable from the description and drawings.

2.6 Amendments made to the description are merely editorial in nature.

2.7 The board concludes that the amendments made comply with the requirements of Article 123(2) EPC.

3. *Novelty (Article 54 EPC)*

Document D3 also relates to ballast circuits for starting and operating gas discharge lamps (column 1, lines 1-5).

3.1 It is common ground that the ballast circuit of claim 1 differs from the one disclosed in document D3 in the specified nature of the diodes 15 and 16, and 70 and 71 respectively, and in that claim 1 further requires that each of the first and second diodes (70, 71) is capable of blocking a reverse voltage substantially equal to the voltage between the positive rail (+HT) and the negative rail (0V).

3.2 The ballast circuit of claim 1 is therefore new.

4. *Inventive step (Article 56 EPC)*

4.1 In document D3, diodes Z1 - Z4, which are illustrated in Fig. 6 of that document using the symbol for Schottky diodes, "protect against DV/DT failures of the MOSFETs internal parasitic diodes" (column 2, line 53 to column 3, line 1). This is achieved by preventing the flow of reactive currents in the output circuit from circulating via the inherently slow recovery body diodes in the MOSFETs. Schottky diodes Z1 and Z2 force reactive currents to flow instead through diodes D1 and D2.

4.2 In the circuit of Figure 5 of the application, the diodes 70 and 71 which are connected in series with MOSFET 9 and 10 respectively, act to block the body diode currents in the MOSFETs 9 and 10 in the same

manner as is described in document D3. However, and more importantly they also act to block the flow of capacitive currents associated with the drain-to-source capacitance of the inactive MOSFET that would otherwise be commutated by the active MOSFET (published application, column 8, lines 19 to 25).

4.3 As explained in paragraphs 2.3 to 2.3.3 above, when the circuit in Fig. 5 operates in its second mode of operation, the voltage at node A oscillates at high frequency between approximately 0V and +HT. In the absence of the series-connected diodes 70 and 71 the charging currents of the drain-to-source capacitance of the MOSFET would be high, because the capacitance has low impedance at high frequency.

4.4 In document D3, the problem of the parasitic capacitance of the MOSFETs is not addressed, and hence the document D3 cannot provide any indication of a possible solution to this problem.

4.5 Moreover, as convincingly explained by the appellant, the Schottky diodes Z1 and Z2 used in document D3 could not withstand a high reverse voltage and would therefore not prevent the parasitic capacitance of the MOSFETs from being charged and discharged, leading thus to important power losses.

4.6 Document D4 recognises the problem of parasitic capacitances of MOSFETs. However, it concerns itself with the possibility of both of a pair of switching elements being ON at the same time (column 2, line 50 to column 3, line 9). Document D4 proposes to couple the switching elements (1, 2) "through their respective

series-connected smoothing choke coils (31, 32) to a capacitor 4 in a low frequency (or DC) portion. Because of this, any sharp change in voltage, for example, which is produced at the opposite terminals (node 75 or 76) of either of the switching elements in consequence of the actuation of the relevant switch is absorbed by the series-connected choke coils and the parallel-connected capacitor, with the result that the otherwise possible direct transfer of the change in the voltage in one of the switching elements to the other switching element is precluded." (column 4, lines 51-62).

Document D4 does not address the problem of avoiding losses owing to the charging currents of parasitic capacitances of a MOSFET.

- 4.7 It follows from the foregoing that neither of the cited documents addresses, and even less suggests a solution to, the problem of losses occurring in lamp ballast circuits on account of high charging currents of the parasitic capacitances of MOSFETs. Therefore, the skilled person could not arrive at the claimed ballast circuit by any combination of the teachings of documents D3 and D4. Consequently, the board judges the invention claimed in claim 1 to involve an inventive step in accordance with Article 56 EPC.

Order

For these reasons it is decided that:

1. The decision under appeal is set aside.
2. The case is remitted to the department of first instance with the order to grant a patent with the following documents:

claims 1 to 12 submitted during oral proceedings

description: pages 1 to 3 and 8 to 10 filed on
28 April 2003,
pages 4, 6, 7, 11 to 16 submitted during
oral proceedings

Figures as originally filed

Registrar:

Chair:

S. Sánchez Chiquero

V. L. P. Frank