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Datasheet for the decision of 23 March 2010

Case Number: T 1436/06 - 3.5.02

Application Number: 00310447.8

Publication Number: 1104110

IPC: H03L 7/081

Language of the proceedings: EN

Title of invention:
Phase-combining circuit and timing signal generator circuit for carrying out a high-speed signal transmission

Applicant:
FUJITSU LIMITED

Opponent:
-

Headword:
-

Relevant legal provisions:
EPC Art. 56, 84, 111(1), 123(2)

Relevant legal provisions (EPC 1973):
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Keyword:
-

Decisions cited:
-

Catchword:
-

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Case Number: T 1436/06 - 3.5.02

D E C I S I O N
of the Technical Board of Appeal 3.5.02
of 23 March 2010

Appellant: FUJITSU LIMITED
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Decision under appeal: **Decision of the Examining Division of the European Patent Office posted 21 March 2006 refusing European application No. 00310447.8 pursuant to Article 97(1) EPC 1973.**

Composition of the Board:

Chairman: M. Ruggiu
Members: G. Flyng
E. Lachacinski

Summary of Facts and Submissions

I. The applicant appealed against the decision of the examining division refusing the European patent application no. 00 310 447.8.

II. In the contested decision, the examining division refused the application on the grounds that

(i) the claims on file were not clear, Article 84 EPC,

(ii) the subject-matter of claim 1 did not involve an inventive step, Article 56 EPC, and

(iii) the description was not in line with Rule 27(1)(c) EPC 1973.

The finding of lack of inventive step was based on the disclosure of document D1: WO98/37656.

III. With the written statement setting out the grounds of appeal, filed with the letter dated 20 July 2006, the appellant submitted a replacement set of claims 1 to 35 and further amended description pages 16, 17, 61 to 69 and 71.

IV. The board summoned the appellant to attend oral proceedings. In an annex to the summons the board made observations on the claims filed with the grounds of appeal.

V. With a letter dated 12 March 2010, the appellant filed a further set of claims 1 to 21 in preparation for the oral proceedings.

VI. Oral proceedings were held before the board on 23 March 2010. The appellant withdrew the set of claims filed with the grounds of appeal and submitted an amended claim 1 to replace claim 1 filed with the letter dated 12 March 2010. The appellant requested that the decision under appeal be set aside and the case be remitted to the department of first instance for further prosecution.

VII. Independent claim 1 filed during the oral proceedings of 23 March 2010 (hereinafter: present claim 1) reads as follows:

"1. A phase-combining circuit (5) for combining three or more cyclic input signals of different phases in accordance with a control signal to output a phase-controlled signal comprising:

a weight signal generating circuit (51) for generating weights according to the control signal;

a weighting circuit for giving the weights to the respective input signals,

wherein the weighting circuit includes a plurality of pairs (501, 502, 504...) of differential transistors of which gates are supplied with the input signals, a plurality of transistors (503, 506, 509...), each connected to a pair of differential transistors, and each of which is supplied with the weight (W1,...) so that a current proportional to the weight flows in it;

and at least one load device (52) including a pair of MOS integration capacitors (521, 522), one (521) connected between a voltage source (Vdd) and each first transistor (501, 504,...) of the pairs of differential transistors and the other (522) connected between the

voltage source (Vdd) and each second transistor (502, 505,...) of the pairs of differential transistors,

in which the load device further includes two cross-coupled pairs of MOS transistors (523, 524 and 525, 526), each pair of MOS transistors being connected in parallel between the voltage source (Vdd) and respective ones of the pairs of differential transistors (501, 502, 504...) so as to form a load, one gate of each pair of MOS transistors being connected to said first transistors (501, 504,...) of the pairs of differential transistors, and the other gate of each pair of MOS transistors being connected to said second transistors (502, 505,...) of the pairs of differential transistors,

and wherein a constant current (I1, I2) is supplied to each of said pairs of differential transistors, so that a high impedance is presented to a differential signal applied to a pair of the differential transistors (501, 502, 504) and a low impedance is presented to an in-phase signal applied to a pair of the differential transistors (501, 502, 504)."

VIII. The appellant argued essentially that the claims as amended did not introduce fresh subject-matter contrary to Article 123(2) EPC and were clear and supported by the description, Article 84 EPC. Furthermore, the invention as claimed was novel and involved an inventive step, Articles 54 and 56 EPC.

Reasons for the Decision

1. The appeal is admissible.

2. Amendments, Article 123(2) EPC

Present claim 1 differs from claim 1 as originally filed essentially in that it specifies that the phase-combining circuit includes at least one load device, and furthermore in that it specifies the features of the weighting circuit and the at least one load device.

The features added to claim 1 were not present in the claims as originally filed, but figures 11 and 13 and the associated description in paragraphs [0074] to [0080] of the application as filed (see the published specification EP 1 104 110 A2) do provide a basis for the subject-matter of claim 1 as amended. For this reason the board finds that the amendments according to present claim 1 do not contravene Article 123(2) EPC.

3. Clarity and support, Article 84 EPC

The board finds that the clarity objections raised in the contested decision against claim 1 have been overcome by the amendments made. In particular:

– The feature "two or more input signals of different phases" has been amended to "three or more cyclic input signals of different phases". With this amendment it is clear that the input signals that are to be combined by the claimed circuit are cyclic in nature and are phase-shifted with respect to one another. Furthermore, the

claimed subject-matter is clearly restricted to the case with three or more input signals. With this limitation it seems to be of no consequence whether single-ended or differential input signals (clocks) are used.

– Claim 1 as amended now consistently refers to a control signal. This control signal corresponds to the phase control code that is input to the weight signal generator circuit 51 in the embodiment of figure 11.

– The expression "all of the input signals having the same polarity of positive or negative", that was objected to in the contested decision, has been deleted from claim 1, thereby overcoming the objection raised.

In summary, the board holds present claim 1 to be clear and supported by the description, Article 84 EPC.

4. Novelty and inventive step, Articles 54 and 56 EPC

4.1 Document D1 is the only prior art document cited in the contested decision. The examining division found that document D1 discloses:

– a phase-combining circuit (560 in figure 6 and the whole of figure 18) for combining four input signals of different phases (1700, 1740, 1710, 1750 in figure 18) in accordance with control signals (1500, 1510 in figure 17) to output a phase-controlled signal (1870, figure 18) comprising:

– a weight signal generating circuit (1530 in figure 17) for generating weights (1590, 1640 in

figure 17) according to the control signal (1500, 1510 in figure 17); and

- a weighting circuit (1800, 1810, 1820, 1830 in figure 18) for giving the weights (1590, 1640 in figure 17 and 1720, 1730 in figure 18) to the respective input signals, wherein
- the weighting circuit includes a plurality of pairs of differential transistors (1800, 1810 and 1820, 1830 in figure 18) of which gates are supplied with the input signals (1700, 1740, 1710, 1750 in figure 18),
- a plurality of transistors (1550 ... 1630 in figure 17), connected to the corresponding pair of differential transistors (1800, 1810 and 1820, 1830 in figure 18), which are supplied with the weight,
- and one integration load circuit (1780, 1790, 1760, 1770, 1860, see figure 18) connected to the plurality of pairs of differential transistors (1800, 1810 and 1820, 1830 in figure 18).

The appellant has not contested these findings and the board sees no reason to disagree with them.

4.2 The board considers furthermore that in the circuit disclosed in figures 17 and 18 of document D1:

- the current that flows in the transistors 1550 to 1630 of figure 17 would be proportional to the weights 1, 2, 3 ... c applied to their gates; and
- there is a load device including a pair of capacitors C1, C2, 1760, 1771, one of which (1760) is connected between a voltage source (ground) and each first transistor 1800, 1820 of the pairs of differential transistors and the other of which

(1780) is connected between the voltage source (ground) and each second transistor 1810, 1830 of the pairs of differential transistors.

4.3 Document D1 does not disclose the features of present claim 1 according to which:

- the capacitors are MOS integration capacitors;
- the load device includes two cross coupled pairs of MOS transistors, each pair of MOS transistors being connected in parallel between the voltage source and respective ones of the pairs of differential transistors so as to form a load, one gate of each pair of MOS transistors being connected to said first transistors of the pairs of differential transistors, and the other gate of each pair of MOS transistors being connected to said second transistors of the pairs of differential transistors; and
- a constant current (I1, I2) is supplied to each of said pairs of differential transistors, so that a high impedance is presented to a differential signal applied to a pair of the differential transistors (501, 502, 504) and a low impedance is presented to an in-phase signal applied to a pair of the differential transistors (501, 502, 504).

Thus, claim 1 is to be considered novel with respect to document D1, Article 54 EPC.

4.4 In its decision, the examining division held that although not explicitly disclosed in Dl, it was clearly obvious to the person skilled in the art that the operational amplifier 1860 comprised in the load circuit (1780, 1790, 1760, 1770, 1860 in figure 18) of

Dl also comprised cross-coupled transistors. In the absence of any evidence supporting this allegation, the board is not in a position to confirm its correctness.

5. With the amendment of claim 1 to include detailed features of the load device that were not comprised in the claims forming the basis of the contested decision, an entirely new situation has been created that was not considered by the department of first instance.

For this reason the board, making use of its power under Article 111(1) EPC, accedes to the appellant's request and remits the case to the department of first instance for further prosecution, in particular for examination of inventive step on the basis of claim 1 filed during the oral proceedings of 23 March 2010.

The present application documents are as follows:

- claim 1 filed during the oral proceedings of 23 March 2010;
- claims 2 to 21 filed with the letter dated 12 March 2010;
- description pages 16, 17, 61 to 69 and 71 filed with the letter dated 20 July 2006;
- the remaining description pages and the drawings filed during the first instance procedure.

Order

For these reasons it is decided that:

1. The decision under appeal is set aside.

2. The case is remitted to the department of first instance for further prosecution.

The Registrar: The Chairman:

U. Bultmann M. Ruggiu