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Datasheet for the decision of 21 November 2008

Case Number: T 0966/06 - 3.4.03

Application Number: 03090388.4

Publication Number: 1422760

IPC: H01L 29/786

Language of the proceedings: EN

Title of invention:
Thin film transistors and organic electroluminescent device using the same

Applicant:
Samsung SDI Co., Ltd.

Opponent:
-

Headword:
-

Relevant legal provisions:
-

Relevant legal provisions (EPC 1973):
EPC Art. 56

Keyword:
"Inventive step (no)"

Decisions cited:
-

Catchword:
-

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Case Number: T 0966/06 - 3.4.03

D E C I S I O N
of the Technical Board of Appeal 3.4.03
of 21 November 2008

Appellant: Samsung SDI Co., Ltd.
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Decision under appeal: **Decision of the Examining Division of the European Patent Office posted 31 January 2006 refusing European application No. 03090388.4 pursuant to Article 97(1) EPC.**

Composition of the Board:

Chairman: R. G. O'Connell
Members: G. Eliasson
U. Tronser

Summary of Facts and Submissions

I. This is an appeal against the refusal of application 03 090 388 for lack of clarity, lack of novelty and added subject matter.

II. The following prior art documents, among others, were cited in the examination procedure:

D12: H.C. Card et al. "Studies of Interface Phenomena at Silicon Grain Boundaries", IEDM 83, pages 198 to 201;

D14: WO 97 45 827 A.

III. At oral proceedings before the board, the appellant applicant requested that the decision under appeal be set aside and a patent granted on the basis of one of a main request or first or second auxiliary request sent with a letter dated 21 October 2008.

IV. Claim 1 of the main request reads as follows:

"1. A method for forming a plurality of thin film transistors using sequential lateral solidification method, wherein each of the thin film transistors comprises an active channel region and the active channel regions of said thin film transistors have the same orientation, wherein primary crystal grain boundaries resulting from the sequential lateral solidification method and being controllable in a position in a polycrystalline silicon formed on a substrate and having an inclined angle of 45° to 135° with respect to a current flow direction in the active

channel regions are arranged such that they do not meet boundaries between the drain regions and the active channel regions of said thin film transistors,

characterised in that

the primary crystal grain boundaries are formed with a width of 1 µm or less and wherein the crystal grain boundaries resulting from the sequential lateral solidification are arranged such that a centre of the closest primary crystal grain boundary is separated from the boundary between a drain region and an active channel region by at least 0.5 µm."

V. Claim 1 of the first auxiliary request reads as follows:

"1. A method for forming a plurality of thin film transistors using sequential lateral solidification method wherein primary crystal grain boundaries resulting from the sequential lateral solidification method and being controllable in a position in a polycrystalline silicon formed on a substrate and having an inclined angle of 45° to 135° with respect to a current flow direction are arranged such that they do not meet boundaries between the drain regions and the active channel regions of said thin film transistors, wherein the active channel regions of said thin film transistors have the same orientation
characterised in that

the primary crystal grain boundaries are formed with a width of 1 µm or less and the crystal grain boundaries resulting from the sequential lateral solidification are arranged such that a centre of the primary crystal grain boundaries is separated from the boundary between a drain region and an active channel region by at least 0.5 µm."

VI. Claim 1 of the second auxiliary request reads as follows (board's emphasis indicating differences with respect to the first auxiliary request):

"1. A method for forming a plurality of thin film transistors using sequential lateral solidification method wherein primary crystal grain boundaries resulting from the sequential lateral solidification method and being controllable in a position in a polycrystalline silicon formed on a substrate and having an inclined angle of 45° to 135° with respect to a current flow direction are arranged such that they do not meet boundaries between the drain regions and the active channel regions of said thin film transistors, wherein the active channel regions of said thin film transistors have the same orientation
characterised in that
the primary crystal grain boundaries are formed with a width of 1 µm or less and the crystal grain boundaries resulting from the sequential lateral solidification are arranged such that a centre of the primary crystal grain boundaries is separated from the boundary between a drain region and an active channel region by at least 0.5 µm, **and**

wherein at least one primary crystal grain boundary is arranged inside the active channel region of the thin film transistor."

VII. Each of the above requests also comprises an independent claim 3 directed to a polycrystalline silicon thin film having features corresponding to those of claim 1 of the respective request.

VIII. The arguments of the appellant applicant can be summarised as follows:

(a) Figure 3A of document D14 showed grain boundaries within the channel which were perpendicular to the current direction. The problem of primary grain boundaries meeting the boundaries between the drain region and the channel region was however not mentioned.

(b) Document D12 investigated theoretically carrier transport and interface state kinetics at grain boundaries of silicon but did not discuss the position of the grain boundaries with respect to the channel. Hence document D12 did not teach keeping the grain boundaries away from the source/channel and drain/channel boundaries.

In particular, from the discussion of Fig. lb of document D12 it appeared that the energy of the conduction band was raised thereby impairing the characteristics of the channel. However, no hint was given that would suggest any disadvantage to placing the grain boundaries at the source/channel and drain/channel boundaries.

Hence the person skilled in the art would not be taught by document Dl2 to avoid placing primary grain boundaries at the drain/channel boundary.

Reasons for the Decision

1. The appeal is admissible.

2. *Inventive Step - Main Request*

2.1 Document D14 was cited in the application and discloses a method of forming a plurality of Thin Film Transistors (TFT) (see Figures 3A and 3B with accompanying text). A plurality of polycrystalline regions is formed in an amorphous silicon layer by the sequential lateral solidification method, ie irradiating the region by laser to melt and resolidify the silicon region and a TFT is formed in each polycrystalline region. Figure 3A illustrates a TFT with one "primary grain boundary" in the channel, ie a grain boundary substantially perpendicular to the current direction in the channel region. The TFTs are intended to be used in applications such as liquid crystal displays which implies that at least a plurality of the TFTs would have their channel regions aligned in the same direction.

2.2 The method of claim 1 of the main request differs from that of document D14 in that

(a) the primary grain boundaries have a width of 1 µm or less, whereas document D14 does not provide any information on this point; and

(b) the centre of the closest primary crystal grain boundary is separated from the boundary between a drain region and the channel region by at least 0.5 µm.

2.3 As regards feature (a), a skilled person taking into account the fact that the typical channel length of a TFT at the priority date of the application would be from about one to several micrometers would as a matter of course seek to restrict the primary grain boundary width to be at least an order of magnitude smaller than the channel length, in order to limit the effects of the primary grain boundary on the on-characteristics of the TFT. The claimed limit of 1 µm or less would thus not only lie within the range contemplated by the skilled person without the exercise of inventive skills but would also lie within that attainable through routine adjustment of the process parameters. It is also noted that the application does not mention any process parameters used for producing a polycrystalline film having grain boundary widths of 1 µm or less (see eg paragraph 0035).

2.4 As to feature (b), placing the closest primary crystal grain at least 0.5 µm from the boundary between the channel region and the drain region, it is undisputed common general knowledge in the art that defects at a pn-junction have detrimental effects on the blocking ability of the pn-junction, since defects may cause leakage current of a reverse-biased pn-junction. Thus,

for this reason alone the skilled person would expect that a primary grain boundary placed at the vicinity of the channel/drain boundary (junction) in a TFT might have negative effects on the blocking capacity of the TFT in the OFF-state.

2.5 Document D12 is a scientific article presenting the results of experimental and theoretical studies of carrier transport phenomena at silicon grain boundaries. It is found that thermoionic-field emission from grain-boundary interface states can be the dominant carrier emission mechanism even at room temperature and moderate doping concentrations (see abstract and page 201, "Conclusions").

As thermoionic-field emission appears when a voltage is applied across the grain --which is the case when a grain boundary would be in the vicinity of a reversed-blocking drain-channel pn-junction, the skilled person learns from document D12 that grain boundaries would have the tendency to emit carriers, ie cause leakage current. This information would thus confirm to the skilled person the importance of placing primary grain boundaries outside of regions subject to high electric fields in order to keep a low leakage current. In the case of a TFT this could mean not only away from the drain-channel boundary, but also preferably outside of the space-charge region formed when the TFT is in the OFF-state. Hence, the skilled person would seek to place the primary grain boundaries at least 0.5 µm from the drain/channel boundary.

2.6 The appellant applicant argued in this connection that since document D12 did not discuss the issue of where

the grain boundaries should be positioned with respect to the channel, it would not teach the skilled person to keep the grain boundaries spaced away from the source/channel and drain/channel boundaries.

The above argument fails to persuade the board, since, as noted above, it is undisputed common general knowledge that defects and crystal imperfections at a pn-junction, such as the drain/channel boundary, can be the cause of leakage current. Therefore, the skilled person would from the onset be inclined to keep primary grain boundaries from crossing the drain/channel boundary. Document D12 merely confirms that grain boundaries indeed behave as defects having interface states acting as traps for majority carriers (page 200, left hand column, first paragraph). When a voltage is applied across a grain boundary, as the case would be if the grain boundary would be in the vicinity of a reverse-biased pn-junction, another mode of carrier conduction, thermoionic-field emission, which was not relevant in bulk conduction, suddenly plays a dominant role (see "Conclusions").

2.7 For the above reasons, in the board's judgement, the subject matter of claim 1 of the main request is not to be considered as involving an inventive step within the meaning of Article 56 EPC 1973.

3. *Inventive Step - First and Second Auxiliary Requests*

The scope of claim 1 of the first auxiliary request is the same as that of the main request, the variation in wording representing differing attempts to overcome potential objections of added subject matter. Claim 1

of the second auxiliary request adds to the method of claim 1 of the first auxiliary request the feature that at least one primary crystal grain boundary is arranged inside the active channel region of the thin film transistor, a feature which is already known from document D14, Figure 3B. It follows that the subject matter of claim 1 of the first and second auxiliary request does not involve an inventive step within the meaning of Article 56 EPC 1973 for the same reasons as given for the main request.

Order

For these reasons it is decided that:

The appeal is dismissed.

Registrar Chair

S. Sánchez Chiquero R. G. O'Connell