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Datasheet for the decision
of 11 May 2010

Case Number: T 0811/06 - 3.5.04

Application Number: 00986480.2

Publication Number: 1247403

IPC: H04N 7/24

Language of the proceedings: EN

Title of invention:
Hardware filtering of input packet identifiers for an MPEG
re-multiplexer

Applicant:
GENERAL INSTRUMENT CORPORATION

Opponent:
-

Headword:
-

Relevant legal provisions:
EPC Art. 54, 56

Relevant legal provisions (EPC 1973):
EPC Art. 113(1)
EPC R. 68(2)

Keyword:
"Inventive step - no (main request)"
"Novelty - no (auxiliary request)"
"Basis of decision - opportunity to comment (yes)"
"Basis of decision - decision reasoned (yes)"

Decisions cited:
T 0939/92, T 0329/04, T 1242/04

Catchword:
See points 4.6 and 4.8

Case Number: T 0811/06 - 3.5.04

D E C I S I O N
of the Technical Board of Appeal 3.5.04
of 11 May 2010

Appellant:	GENERAL INSTRUMENT CORPORATION 101 Tournament Drive Horsham Pennsylvania 19044 (US)
Representative:	Cooper, John Murgitroyd & Company 165-169 Scotland Street Glasgow G5 8PL (GB)
Decision under appeal:	**Decision of the Examining Division of the European Patent Office posted 2 January 2006 refusing European application No. 00986480.2 pursuant to Article 97(1) EPC 1973.**

Composition of the Board:

Chairman:	F. Edlinger
Members:	A. Dumont
	B. Müller

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Summary of Facts and Submissions

I.   The appeal is directed against the decision to refuse
        European patent application 00 986 480.2, published as
        WO 01/45418 A1.

II.   The application was refused on the ground that the
        subject-matter of claim 1 according to all requests
        filed during oral proceedings on 11 October 2005 lacked
        an inventive step starting from the prior art disclosed
        in:

        D2: US 5,835,493 A.

III.   The appellant requested in writing that the decision
        under appeal be set aside and a patent be granted on
        the basis of the main and auxiliary requests on file,
        i.e. in the version filed on 11 October 2005. The
        appellant further requested reimbursement of the appeal
        fee arguing that the examining division had committed a
        substantial procedural violation, and requested oral
        proceedings *in lieu* of any adverse decision.

IV.   In an annex to the summons to oral proceedings the
        board expressed the preliminary opinion that the
        subject-matter of claim 1 according to the main request
        lacked an inventive step over D2 and common general
        knowledge, that the subject-matter of claim 1 according
        to the auxiliary request lacked novelty over D2, and
        that the board could not see a substantial procedural
        violation that would justify reimbursement of the
        appeal fee.

V.   In a letter dated 11 March 2010 the appellant informed
       the board that he would not be represented at the oral
       proceedings and requested a decision according to the
       state of the file.

VI.   Oral proceedings took place on 11 May 2010.

VII.   Claim 1 according to the main request reads as follows.

       "An input processing device for use in a remultiplexing
       module (100) that processes input packet data,
       comprising:
       an input interface (118) that receives the input packet
       data;
       an input processor (120) coupled to the input interface
       (118) to receive input packet data therefrom and write
       data to a packet buffer;
       a packet identifier table (122) coupled to the input
       processor; and
       characterised in that the packet identifier table (122)
       is divided into two separate tables (300, 322) that act
       interchangeably as an active packet identifier table
       and a pending packet identifier table, the current
       active packet identifier table containing values for
       use by the input processor (120) to select packets for
       storage in an input packet data stream and the current
       pending table containing values that can be modified by
       a host processor (114) while the active table is being
       used by the input processor, the statuses of the two
       tables being switchable to turn the pending table into
       the current active table and the active table into the
       current pending table."

VIII.   Claim 1 according to the auxiliary request reads as
        follows.

        "An input processing device for use in a remultiplexing
        module (100) that processes input packet data,
        comprising:
        a plurality of input interfaces (118) each of which
        receives one of a corresponding plurality of data
        transport streams, each of which contains input packet
        data;
        a corresponding plurality of input processors (120)
        each coupled to a respective one of the input
        interfaces (118) to receive input packet data from a
        respective data transport stream; and
        a corresponding plurality of packet identifier tables
        (122) each of which is coupled to a respective input
        processor (120);
        characterised by at least one of the plurality of input
        processors (120) being arranged to extract packet data
        from the respective data transport stream to be output
        in at least one output data stream and being further
        arranged to write said extracted packet data to a
        respective packet buffer (104)."

IX.   The reasoning of lack of inventive step in the decision
        under appeal may be summarised as follows. There are
        many examples in the prior art, in many different
        fields, of the use of "ping-pong" memory architectures,
        for example by using different memory areas in
        computers to provide instantaneous screen changes. Thus
        the features of claim 1 not anticipated by D2 represent
        an obvious use of a well-known technique, the
        advantages of which technique making it quite suited in
        the context of the apparatus of D2.

X.   The appellant's arguments may be summarised as follows:

-       The RAM and the buffer according to D2 do not store
        active and pending tables according to the present
        invention. There is also no evidence as to how PID
        values stored in the RAM or the buffer according to
        D2 are updated and overwritten to form a table.

-       The common general knowledge of ping-pong memory
        architectures is from a field remote from the field
        of MPEG data multiplexing. Arriving at the two-part
        table according to the invention would thus result
        from an *ex-post facto* analysis, which is not
        allowable.

-       D2 does not address the inability at the priority
        date of the application to multiplex multiple output
        streams from multiple input streams, so that the
        provision of an architecture suitable for
        multiplexing such multiple output streams was
        inventive.

-       The examining division failed to produce documentary
        evidence of common general knowledge relating to
        double buffering and ping-pong architecture in the
        context of look-up tables, which was disputed by the
        appellant. This deprived the appellant of the
        opportunity to present comments in relation to
        anything other than a bald assertion of "common
        general knowledge" and prevented him to formulate a
        cogent response. This also led to an insufficiently
        reasoned decision within the meaning of Rule 68(2)
        EPC 1973.

Reasons for the Decision

1.   The appeal is admissible.

2.   Main request

2.1   It is uncontested that a device according to the
        preamble of claim 1 is known from D2, where the packet
        identifier (PID) table is stored in PID RAM 220 and
        downloaded into buffer 222 (see figure 3), which
        corresponds to the active identifier table according to
        the present invention. The table is used to identify
        and select input packets in the transport stream, which
        are written ("transferred") to an output buffer (228)
        depending on the result of the comparison of their PID
        values with those stored in the active table (see D2,
        column 7, lines 1 to 15; column 8, lines 1 to 10 and
        column 13, line 55 to column 14, line 23).

2.2   D2 encompasses the use of a single (active) table. The
        provision of two separate and interchangeably acting
        (active and pending) tables according to claim 1 is not
        known from D2.

2.3   The technical problem to be solved by the provision of
        such active and pending tables is to allow dynamic
        reconfiguration of the device without interrupting the
        operation of the input processor. The content of the
        pending table is modified whereas the active table is
        used for packet selection. The host processor may then
        choose to put the pending table into effect simply by
        modifying the value of a control bit, thereby
        instantaneously switching the statuses of the two

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tables (see paragraphs [0017] and [0019] of the
description in the present application).

2.4   The board is satisfied that "ping-pong" memory
        architectures were commonly known for increasing the
        throughput of data streams in different technical
        fields. As mentioned by the examining division, one
        notable example could be found in computer graphics,
        where an instantaneous screen change is achieved by
        changing the address of the memory area from which the
        screen data is fetched. More generally, "ping-pong"
        denominates an architecture allowing data to be written
        to a "ping" memory while data is read from a separate
        "pong" memory, prior to interchanging the role of the
        "ping" and "pong" memories.

2.5   D2 relates to the same technical field of MPEG
        remultiplexers as the present invention, where both
        constraints about data throughput and the need for
        regular reconfiguration have to be taken into account.
        The skilled person starting from D2 and confronted with
        the above problem (see point 2.3) would therefore have
        looked for a reconfiguration scheme preserving
        throughput as much as possible.

2.6   The *raison d'être* of a ping-pong architecture is to
        instantaneously allow two memory areas to be
        interchanged with essentially no interruption in the
        operation. Therefore the person skilled in the art, in
        view of his common general knowledge, would have
        considered modifying the device according to D2 and
        implementing a ping-pong scheme so as not to affect the
        operation of the device during reconfiguration. As a
        result, changing the statuses of the active and pending

tables as specified in the characterising portion of
claim 1, resulting in replacing an active table by a
previously downloaded pending table, does not show an
inventive step.

2.7   The technical field of computer graphics may be remote
       from the field of MPEG data remultiplexing. However, it
       was mentioned by the examining division merely as an
       example and the technical problem with which the
       skilled person was confronted, starting from D2,
       relates to dynamic reconfiguration of data stored in a
       buffer. This is a problem which may occur in many areas
       of digital data processing, for instance also in the
       technical field of computer graphics. Ping-pong memory
       architectures are so widely known that the skilled
       person would have contemplated their use in any field
       where a fast memory update is desirable, thus also in
       MPEG remultiplexers with reconfigurable PID table(s).

2.8   As a result, the board judges that the subject-matter
       of claim 1 according to the main request lacks an
       inventive step over D2 and the common general knowledge
       of the skilled person.

3.   Auxiliary request

3.1   Claim 1 of the auxiliary request is directed to a
       device with a plurality of input processors. It is
       uncontested that a device according to the preamble of
       claim 1 was known from D2. The remultiplexer according
       to D2 assembles one or more input transport streams,
       using one or more modules according to figure 3, into
       one single output transport stream (see for instance
       column 1, lines 15 to 24 and column 8, lines 39 to 43).

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3.2   The characterising portion of claim 1 sets out that at
       least one input processor is arranged to extract packet
       data from the respective data transport stream to be
       output in at least one output data stream and to write
       said extracted packet data to a respective packet
       buffer. Claim 1 thus essentially sets out the operation
       within (at least) one input processor, which is the
       same as in D2, in which the data is written in output
       buffer (228) to be assembled and outputted in (at least)
       one output data stream.

       According to the description (see for instance
       paragraph [0024]), the generation of multiple output
       data streams is a feature of the output processor
       according to figure 4. Claim 1 does not contain a
       corresponding feature. Claim 1 also does not set out
       features, neither explicitly nor implicitly, which
       could determine or influence the routing of packet data
       to different output streams in an output processor.
       Thus no feature of the input processing device
       according to claim 1 makes it particularly suitable for
       a use with multiple output streams, contrary to the
       appellant's contention. The board thus disagrees with
       the appellant arguing that the present invention is
       distinguished from the prior art in that it is suitable
       to multiplex multiple output streams.

3.3   As a result, all the features of the input processing
       device of claim 1 according to the auxiliary request
       being disclosed in D2, its subject-matter lacks novelty
       over D2.

4.   Alleged substantial procedural violation

4.1   The examining division asserted in the refusal of claim
        1 of the main request that the division of a memory in
        two interchangeable separate areas according to the
        characterising portion of claim 1 was known in many
        fields, for instance as a "ping-pong" memory
        architecture and was thus common general knowledge.

4.2   The appellant argues that the examining division, by
        not providing a prior art document in support of this
        assertion, failed to sufficiently reason its decision,
        and prevented him from formulating a cogent response.
        The question arises as to whether the behaviour of the
        examining division in the proceedings up to refusal
        deprived the applicant of the right to be heard
        (Article 113(1) EPC 1973), and whether the decision was
        sufficiently reasoned (Rule 68(2) EPC 1973).

4.3   Decision T 939/92 (OJ EPO 1996, 309) referred to by the
        appellant in the statement of grounds of appeal
        (followed for instance in T 1242/04, OJ EPO 2007, 421;
        see point 9.2 of the reasons) sets out that
        Article 54(2) EPC 1973 does not limit the state of the
        art to written disclosure in specific documents. Rather
        it defines it as including all other ways ("in any
        other way") by which technical subject-matter can be
        made available to the public. Therefore, the absence of
        a reference to a particular document does not mean that
        there is no state of the art, as this could reside
        solely in the relevant common general knowledge, which,
        again, may be in writing, i.e. in textbooks or the like,
        or be simply a part of the unwritten "mental furniture"
        of the notional "person skilled in the art".

It is true, and the board agrees with the appellant in
this respect, that in the case of any dispute as to the
extent of the relevant common general knowledge this,
like any other fact under contention, has to be proved,
for instance by documentary or oral evidence (see also
T 329/04, not published in OJ, point 45 of the reasons).

4.4   According to the minutes of the oral proceedings held
        before the examining division, the applicant accepted
        that conventional structures known as "double-
        buffering" or "ping-pong" memory architecture might be
        used to increase the throughput of data streams. The
        board thus deduces that the applicant did not dispute
        that a ping-pong memory architecture and its benefit
        were common general knowledge. By contrast, the
        appellant stated that he was unaware of an example in
        the context of look-up tables (see the paragraph
        bridging pages 1 and 2 of the minutes).

4.5   Claim 1 of the refused main request sets out separate
        (active and pending) tables for selecting packets and
        does not expressly set out look-up tables. The last
        paragraph on page 4 of the decision under appeal refers
        to examples of ping-pong memory architectures with
        separate memory areas in general and also does not
        specifically refer to the use of such areas as look-up
        tables.

4.6   The device of D2 uses a memory containing a single
        table (operating indeed in practice as a look-up table)
        to select data packets (see also point 2.1 above). This
        was not contested by the appellant. The question
        whether a person skilled in the art would have combined

the teaching of D2 with the (uncontested) common general knowledge of a ping-pong architecture having two interchangeable memory areas is a matter of judgment. Documentary evidence for the feature of ping-pong architecture "in the context of look-up tables" was thus not necessary, and the examining division was not required to provide documentary evidence for their argumentation.

4.7   In view of the above, and since the reasoning in the decision only reflects issues which have been debated in the oral proceedings (which the appellant did not contest), the appellant was not deprived of an opportunity to present comments on the issues relevant to the outcome of the case in the proceedings up to refusal (*cf.* Article 113(1) EPC 1973).

4.8   Rule 68(2), first sentence, EPC 1973 aims to put the appellant in a position to ascertain the reasons for the decision in order to defend his rights, in particular by setting out grounds of appeal, and the board to exercise its power of review of the legality of the decision. As explained in the foregoing, the reasoning in the decision under appeal (see in particular the last paragraph on page 4) built on facts disclosed in D2 and uncontested common general knowledge to conclude that the subject-matter of claim 1 lacked an inventive step. The argument qualified by the appellant as a bold assertion of "common general knowledge" did not prevent him from understanding the reasoning in the decision and from formulating counter-arguments in the statement of grounds of appeal. Therefore, the decision is also considered to be sufficiently reasoned.

4.9   As a result, the examining division did not commit a
         substantial procedural violation and the appellant's
         request for reimbursement of the appeal fee is not
         allowable.

5.   In conclusion, none of the appellant's requests being
         allowable, the appeal must be dismissed.

Order

For these reasons it is decided that:

The appeal is dismissed.

The Registrar   The Chairman

L. Fernández Gómez   F. Edlinger