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Datasheet for the decision of 11 December 2008

Case Number: T 0786/06 - 3.5.01

Application Number: 96936776.2

Publication Number: 0870241

IPC: G06F 13/00

Language of the proceedings: EN

Title of invention:
Protocol for communication with dynamic memory

Patentee:
RAMBUS INC.

Opponent 02:
MICRON EUROPE LTD.

Headword:
Dynamic memory/RAMBUS

Relevant legal provisions:
-

Relevant legal provisions (EPC 1973):
EPC Art. 100(a), (b), 106, 107, 108
EPC R. 64(b)

Keyword:
"Examination of appeals - admissible (yes)"
"Maintenance of patent as amended - third auxiliary request (yes)"

Decisions cited:
J 0010/07

Catchword:
-

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Case Number: T 0786/06 - 3.5.01

D E C I S I O N
of the Technical Board of Appeal 3.5.01
of 11 December 2008

Appellant: (Opponent 02)
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Decision under appeal: **Decision of the Opposition Division of the European Patent Office posted 14 February 2006 rejecting the opposition filed against European patent No. 0870241 pursuant to Article 102(2) EPC 1973.**

Composition of the Board:

Chairman: S. Steinbrener
Members: S. Wibergh
G. Weiss

Summary of Facts and Submissions

I. This is an appeal against the decision of the opposition division taken on 8 December 2005 to reject the opposition filed by Opponent 02 (Micron Europe Ltd, appellant) against European Patent No. 0 870 241. Opponent 01 (Infineon Technologies AG) had withdrawn its opposition on 23 March 2005.

II. The following documents will be referred to:

E9: Synchronous DRAM MT48LC4M4R1(S) and MT48LC2M8S1(S), data sheet, Micron Semiconductor Inc., 1994, pp. 2-1 to 2-84;
E18: JP-A-63 239676 (& English translation thereof);
E19: WO-A-91/16680.

III. According to the decision appealed, the invention as defined in the independent claims 1, 6, 11 and 15 was new and involved an inventive step with respect to the cited prior art, and had been described in a sufficiently clear and complete manner.

IV. By letter dated 12 April 2006 and received on the same day, the appellant filed a "Notice of Appeal against, in its entirety, the decision dated 8th December 2005". In its grounds of appeal, received on 26 June 2006, it requested revocation of the patent in its entirety.

V. By letter dated 21 November 2006, the respondent requested that the appeal be rejected as inadmissible. As a matter of precaution in order to provide a full response it requested that the appeal be dismissed or,

on an auxiliary basis, that five sets of amended claims be considered.

VI. In a communication, the Board issued a summons to oral proceedings and set out its provisional opinion on the appeal. Considering the appeal to be admissible, it noted in particular that the opposition division's reasoning as to novelty and inventive step relied on a specific interpretation of the expression "data transfer operation" in the claims as granted, which expression in the Board's view merely meant that some data were transferred. Comments were also made on the expression "interleave pattern" in claim 16 as granted.

VII. Oral proceedings before the Board were held on 10 and 11 December 2008. In the course of the proceedings the respondent presented three auxiliary requests replacing all previous auxiliary requests. The first auxiliary request concerned amendments to independent claims 1, 6 and 11, the second auxiliary request further amendments to claims 1 and 6, and the third auxiliary request was directed to claims 15 to 17 as granted, renumbered 1 to 3, all other claims being cancelled. The latter request also comprised a new description, consisting of pages 2 to 4 (based on the patent specification as published) and pages 7 to 54 (based on the annex to the communication under Rule 51(4) EPC 1973 dated 8 May 2002).

VIII. The appellant requested that the decision under appeal be set aside and the European patent be revoked.

The respondent requested that the appeal be dismissed (main request) or in the alternative that the patent be

maintained as amended on the basis of claims 1, 6 and 11 submitted at the oral proceedings and claims 2 to 5, 7 to 10 and 12 to 17 as granted (auxiliary request I), or on the basis of claims 1 and 6 submitted at the oral proceedings and claims 2 to 5, 7 to 10 and 15 to 17 as granted (auxiliary request II), or on the basis of claims 1 to 3 submitted at the oral proceedings before the Board (auxiliary request III).

IX. Claim 6 of the respondent's *main request,* ie for the patent as granted, reads:

"A memory device for storing data and performing data transfer operations, the memory device comprising:
a memory for storing data; and
control circuitry coupled to a bus,
wherein the control circuitry is configured to read control information carried on the bus,
wherein the control information includes data that specifies a data transfer operation and a first address, [*]
wherein the memory device is configured to perform the specified data transfer operation on data stored in the memory beginning at the first address,
wherein the memory device is configured to perform the specified data transfer operation on data stored beginning at additional locations specified in address information carried over the bus until detecting a terminate indication on the bus,
wherein the memory device ceases to perform the data transfer operation at a time that is based on the time at which the terminate indication is detected."

X. The respondent's *first auxiliary request* adds to claim 6 as granted the wording "wherein the data transfer operation is either one single READ or one single WRITE operation" inserted at the location indicated by an asterisk [*] in the preceding paragraph.

XI. Claim 6 according to the respondent's *second auxiliary request* contains the amendment introduced with the first auxiliary request and, immediately following it, the insert "and wherein the control information does not contain data transfer size information".

XII. Claim 1 of the respondent's *third auxiliary request* is identical with claim 15 as granted. It reads:

"A memory controller configured to maximize usage of a bus that connects the memory controller to one or more memory devices, the memory controller comprising:
an output unit coupled to a control unit and to the bus,
wherein the control unit is configured to select an interleave pattern based on requests received for a plurality of data transfer operations,
wherein the control unit is further configured to perform the following steps for each data transfer operation of the plurality of data transfer operations;
transmitting control information through the output unit to the bus, wherein the control information specifies the data transfer operation;
determining how much time must elapse between transmission of the control information and the start of the data transfer operation to provide the interleave pattern; and
transmitting a start indicator through the output unit to the bus,

wherein the start indicator specifies when the data transfer operation is to begin."

XIII. At the end of the oral proceedings the Board announced its decision.

Reasons for the Decision

1. *Admissibility of the appeal*

1.1 Articles 106 to 108 EPC 1973 are applicable (see in particular J 10/07, OJ EPO 2006,567, point 1 of the reasons).

1.2 Rule 64 EPC 1973 stipulates that the notice of appeal shall contain a statement identifying the decision which is impugned and the extent to which amendment or cancellation of the decision is requested. The respondent has argued that the present appeal is inadmissible because the notice of appeal did not contain such a request.

1.3 The notice of appeal indicates that it is "against, in its entirety, the decision" but contains no explicit request for revocation of the patent. This request is however implicit for the following reasons. By filing the appeal, the appellant expressed its desire that the decision under appeal be replaced, ie that the patent be either revoked or maintained in amended form. The second alternative was however not open to the appellant since an opponent cannot decide in what form a patent is to be examined (cf Article 113(2) EPC 1973). Thus, the only possible request was revocation of the

patent. No ambiguity being possible, the appeal must be considered admissible (in this context see also the decisions cited in "Case Law of the Boards of Appeal of the European Patent Office", 5th edition 2006, VII.D.7.4.1(b)).

The respondent's main request

2. *The invention according to claim 6*

Claim 6 is directed to a memory device for storing data and performing data transfer operations. It comprises a memory and control circuitry coupled to a bus. Control information arriving over the bus contains a first memory address and an indication whether data are to be written into the memory or read out of it. The desired operation starts at the first address and continues at additional locations specified in address information carried over the bus. A terminate indication marks the end of the data operation.

3. *The prior art*

3.1 E9 is a data sheet describing synchronous DRAM devices produced by Micron Semiconductor, Inc. Each page carries at the bottom the indications "REV. 4/94", "© 1994" and, at the top, "ADVANCE". The respondent argued at the oral proceedings before the Board that the word "ADVANCE" suggested that the data sheet might not have been publicly available at the date of priority (19 October 1995). The appellant, while not being able to explain the meaning of this word, submitted that the two dates printed on the document made it clear that it had been published in 1994.

3.2 The Board notes that E9 is a document issued by a company belonging to the same group as the appellant company. It may therefore be thought that the appellant, if anyone, should be aware of the particulars of its own publication. However, the respondent raised the point concerning the indication "ADVANCE" only at the oral proceedings before the Board, although the document had been on file since the beginning of the opposition proceedings and had been extensively referred to in the decision under appeal. Thus the appellant, having been taken by surprise, cannot be criticised for not having been able to clarify it. The word remaining unexplained, the Board must weigh its importance against the two dates indicating that the document was available about a year before the priority date. Even if "ADVANCE" might relate to a preliminary specification or "advance" information for potential users, the copyright date in particular strongly suggests that the document was intended to be distributed to the public and was, in fact, available in 1994. Judging that, in the absence of any further substantiation to the contrary, two clear indications are more relevant than one obscure, the Board decides that E9 is prior art.

3.3 E9 is mainly concerned with burst commands. Fig. 1 (on p. 2-8), headed "READs INTERRUPTED BY READs", shows ("Case 1") how a first read command "READ Cm" is followed by a second read command "READ Cn" appearing two clock cycles later. The resulting output is a series of data packets "DOUT m1 DOUT m2 DOUT n1 DOUT n2 DOUT n3 DOUT n4", ie two data packets associated with the first read command followed by four data packets

associated with the second command. A burst can be terminated with a burst terminate command, another burst command or a precharge command (p. 2-14, top left). The read command is shown on p. 2-15. Besides the Column Address Strobe, it contains in particular column address bits (A0-A9) and a Write Enable bit.

4. *Novelty*

4.1 The parties agree that the meaning of the expression "data transfer operation" in claim 6 is crucial for the question of novelty.

The appellant has argued that this expression can be understood as merely indicating whether the memory is to be read or written. With this interpretation the claimed memory device was not new. E9 also disclosed that the control information included data that specified a data transfer operation (Write Enable) and a first address (A0-A9). The specified data transfer operation (READ) was performed on data stored in the memory beginning at the first address and subsequently on data stored beginning at additional locations specified in address information carried over the bus (interrupting read commands) until detecting a terminate indication on the bus (a burst terminate or precharge command). The data transfer operation ceased at a time that was based on the time at which the terminate indication was detected (after a certain delay).

The respondent has argued that the expression "data transfer operation" has a more limited meaning in claim 6. The skilled person would therefore recognize

that E9 described not one data transfer operation but several, each associated with its own read command. The interrupted and interrupting read bursts shown in fig. 1 were thus in fact two data transfer operations. The invention was different in that it concerned a single data transfer operation preceded by a single set of control information followed by additional addresses.

The opposition division, faced with basically the same arguments, decided that the invention was new (decision, points 2.1 and 2.2). It held that it could not be assumed that in the prior art the original data transfer operation was "continued" at the additional locations after an interrupting command.

4.2 The Board, however, disagrees with the opposition division and finds that the appellant has the stronger arguments. The expression "data transfer operation" is normally self-explaining and applicable to any data transmission. Claim 6 naturally limits its meaning to bus transfers to or from a memory device, but to assume anything more specific about such a general expression without an explicit definition in the description would be arbitrary. The Board therefore sees no reason for not interpreting it in its usual general sense. It follows that it must be regarded as covering in particular the data transfer operation resulting as a consequence of a combination of an interrupting and an interrupted read command as shown in E9.

The opposition division held that the interrupted command is not "continued" at the additional location defined by the interrupting command. If "continued" is understood as referring to consecutive addresses the

opposition division is naturally right, but claim 6 does not require the addresses to be consecutive. If "continued" does not refer to addresses, the argument seems merely to repeat the view that the interrupted and interrupting commands are two separate, successive commands rather than a single one. In either case the reasoning fails to convince.

4.3 Hence, the only difference between the invention and the prior art is the actual wording used to define the memory device. Whereas claim 6 mentions a "data transfer operation", E9 refers to interrupting and interrupted READ commands. Article 54 EPC 1973 states that an invention "shall be considered to be new if it does not form part of the state of the art". It is thus the technical subject-matter of a claim which has to be compared with the technical subject-matter described in a prior art document. If there is identity of subject-matter there is no novelty, whether or not the claim and the prior art document employ identical wordings. In the present case the memory device as defined in claim 6 has been found to have the same structure and perform the same functions as the DRAM in E9. It is therefore not new (Article 54 EPC 1973).

The respondent's first auxiliary request

5. The claims according to respondent's first auxiliary request were filed on the second day of the oral proceedings before the Board. The appellant has pointed out that since the novelty of the invention was questioned in the summons to the oral proceedings, the respondent could have submitted these claims within the period indicated in the summons (ie up to two months

before the hearing). To file them in the oral proceedings was therefore inadmissibly late. The Board, however, considers that the amendments are mainly of a clarifying nature so that the appellant, after being given the time required to study them, was able to discuss the request.

6. Claim 6 has been amended to include the feature that "the data transfer operation is either one single READ or one single WRITE operation".

7. The appellant has questioned the basis for the amendment, arguing that the only instance of the word "single" occurs in the description of the prior art in paragraph [0042]. There is however no need for the Board to go into this issue since the amendment does not overcome the objection against the main request. According to the Board's findings above, the expression "data transfer operation" covers the data transfer resulting from a combination of an interrupting and an interrupted read command as described in E9. In other words, the Board finds that "one single READ operation" is indistinguishable from a single operation of combined READs. It follows that also the subject-matter of claim 6 of the first auxiliary request is not new (Article 54 EPC 1973).

The respondent's second auxiliary request

8. The claims according to respondent's second auxiliary request were filed during the oral proceedings before the Board but are admitted for the reasons given in connection with the first auxiliary request (see point 5 above).

9. Claim 6 according to the second auxiliary request contains the amendment introduced with the first auxiliary request and additionally the limitation that "the control information does not contain data transfer size information".

10. The appellant has argued that the additional feature is also known from the prior art since the read command in E9 contains no data transfer size information (cf "READ COMMAND" at p. 2-15), this information already being present in the mode register (cf p. 2-7 "BURST MODE"). The respondent, on the other hand, is of the opinion that the stored transfer size information described in E9 is control information which is necessarily referred to, else the transfer size would be undefined.

11. The Board notes that according to claim 6 "the control information includes data that specifies a data transfer operation and a first address". This definition applies to the read command in E9 (cf p. 2-15: the operation is a READ because Write Enable is not set; column addresses are specified on the lines A0-A9) but does not apply to the data in the mode register. Since the read command undisputedly does not contain data transfer size information, the additional feature is indeed known from E9. The subject-matter of claim 6 is thus also not new (Article 54 EPC 1973).

The respondent's third auxiliary request

12. The respondent's third auxiliary request is directed to claims 15-17 as granted, renumbered 1-3. These claims concern a memory controller configured to maximize

usage of a bus that connects the memory controller to one or more memory devices. The appellant has objected to them under Article 100(a) and (b) EPC 1973.

13. Claim 1 refers to an "interleave pattern". The word "interleave" is defined in the description (paragraph [0038]) in the following way: "Interleave refers to the relative ordering of data, requests and control signals that are associated to multiple transactions". The claim thus requires that it be possible to select the *order* of signals. Delays that are not long enough to influence the signal order do not create an interleave pattern.

14. Starting with the objection that the invention has not been disclosed in a manner sufficiently clear and complete for it to be carried out be a person skilled in the art (Article 100(b) with 83 EPC 1973), the Board notes that the appellant's argument is based on the rather general allegation that it is not disclosed how to determine the time that should elapse between transmission of the control information and the start of the data transfer operation in order to provide the interleave pattern. The question before the Board is if the skilled person would have been able to determine this time without exercising inventive skill.

Claim 1 states that the memory controller is configured to "maximize" usage of the bus. The respondent has explained that this should merely be understood as improving, rather than optimizing, usage as compared with a non-interleaved system, a reading the Board accepts. What the skilled person should be able to do is thus merely devise *any* rule for determining a delay

time resulting in an interleave pattern which is improved in some respect compared with a non-interleaved system. Since this requirement is not very severe and the appellant has not specified any particular difficulty that would have to be overcome, the Board is of the opinion that a skilled person would be able to carry out the invention on the basis of the information provided in the patent-in-suit (cf for example appendices B and C).

15. The appellant has further argued that the invention is not new over the prior art known from E19 or E18 (Article 100(a) with 54 EPC 1973).

15.1 The invention contains a control unit "configured to select an interleave pattern based on requests received for a plurality of data transfer operations". E19 discloses a control unit transmitting transaction requests to a slave (DRAM), wherein the control unit can determine the number of bus cycles between a request and the corresponding data transfer (p. 15, l. 3 to p. 16, l. 7). Since this delay can be used for additional requests, E19 can be said to disclose the selection of an interleave pattern. However, the delay is programmed into the DRAM (p. 23, l. 4-6). The Board can therefore not see that the pattern selection is based on requests received for a plurality of data transfer operations, as required by claim 1.

It follows that the subject-matter of claim 1 is new with respect to E19. The appellant has not argued that the invention was obvious from this document, nor is such an argument apparent to the Board.

15.2 E18 describes a dual port memory used to display graphics on a cathode ray tube. The number of clock cycles required from the activation of the memory to the start of the data transfer operation is variable (p. 21, l. 12-17 of the English translation).

The output signal can be delayed, but it is not apparent to the Board that any signals are interleaved. Furthermore, as the opposition division noted, the variable delay is not based on requests received for a plurality of data transfer operations.

The appellant has argued that read requests to the memory are sequentially arranged in E18 (grounds of appeal, p. 19). In the Board's judgment this is however not an "interleave pattern" in the sense of the patent-in-suit (see point 13 above).

Hence, the subject-matter of claim 1 is new also with respect to E18. Again, the appellant has not argued that the invention was obvious from this document, nor is such an argument apparent to the Board.

16. It follows that the patent should be maintained on the basis of the claims of the third auxiliary request and the correspondingly adapted description.

Order

For these reasons it is decided that:

1. The decision under appeal is set aside.

2. The case is remitted to the department of first instance with the order to maintain the patent as amended in the following version:

Claims:

1-3	submitted as auxiliary request III at the oral proceedings before the Board;

Description:

pages 2-4 and 7-54	filed at the oral proceedings before the Board

Drawings:

as granted.

The Registrar: The Chairman:

T. Buschek S. Steinbrener