BESCHWERDEKAMMERN DES EUROPÄISCHEN PATENTAMTS

BOARDS OF APPEAL OF THE EUROPEAN PATENT OFFICE

CHAMBRES DE RECOURS DE L'OFFICE EUROPEEN DES BREVETS

Internal distribution code:
(A) [ ] Publication in OJ
(B) [ ] To Chairmen and Members
(C) [ ] To Chairmen
(D) [X] No distribution

Datasheet for the decision of 26 November 2008

Case Number: T 0454/06 - 3.5.02

Application Number: 01942252.6

Publication Number: 1307966

IPC: H03K 19/177

Language of the proceedings: EN

Title of invention:
Secure programmable logic device

Applicant:
ATMEL CORPORATION

Headword:
-

Relevant legal provisions:
EPC Art. 123(2)

Keyword:
"Added subject-matter (yes)"

Decisions cited:
-

Catchword:
-

Europäisches Patentamt | European Patent Office | Office européen des brevets

Beschwerdekammern | Boards of Appeal | Chambres de recours

Case Number: T 0454/06 - 3.5.02

D E C I S I O N
of the Technical Board of Appeal 3.5.02
of 26 November 2008

Appellant: ATMEL CORPORATION
2325 Orchard Parkway
San Jose, California 95131 (US)

Representative: Käck, Jürgen
Kahler Käck Mollekopf
Vorderer Anger 239
D-86899 Landsberg/Lech (DE)

Decision under appeal: **Decision of the Examining Division of the European Patent Office posted 25 November 2005 refusing European application No. 01942252.6 pursuant to Article 97(1) EPC 1973.**

Composition of the Board:

Chairman: M. Ruggiu
Members: M. Rognoni
E. Lachacinski

Summary of Facts and Submissions

I. The appellant (applicant) appealed against the decision of the examining division refusing European application No. 01 942 252.6.

II. In the decision under appeal, the examining division held, *inter alia*, that the subject-matter of claim 1 filed with a letter dated 17 August 2005 did not involve an inventive step within the meaning of Article 56 EPC.

III. With the statement of grounds of appeal dated 14 March 2006, the appellant filed amended claims 1 to 4 and requested that the decision of the examining division be set aside and a patent be granted on the basis of the enclosed amended claims 1 to 4, or, if these claims could not be allowed, on the basis of the auxiliary request defined at the end of the statement of grounds of appeal as follows:

"Appellants request to allow claim 1, in which as a further amendment the word "chip" is added in line 23 so that it reads "said security bit (24) has a second state in which only a **chip** erase command can be communicated ..... ".

IV. In a communication dated 18 July 2008 accompanying the summons to oral proceedings, the Board informed the appellant that it was doubtful whether the amended claim 1 complied with Article 123 (2) EPC and that this question would have to be addressed in oral proceedings before the Board.

V. The appellant did not make any submission in reply to the Board's communication, nor did he attend the oral proceedings, which were held as scheduled on 26 November 2008.

VI. Claim 1 according to the appellant's main request reads as follows:

"A secure programmable logic integrated circuit system, comprising:

a programmable logic device (21) in communication with external pins (29); and

a configuration memory device (23), the configuration memory device storing configuration data for programming a configuration of said programmable logic device (21) via a data transfer connection (27),

wherein said configuration memory device (23) includes a security bit (24); and

said security bit has a first state in which configuration data may be programmed and read-back through said external pins (29);

characterized in that

said programmable logic device (21) is integrated on a first chip;

said configuration memory device (23) is integrated on a second chip;

said first and second chips are mounted on a multi-chip module (25) having said external pins (29);

said data transfer connection (27) is an inter-chip connection internal to said multi-chip module (25);

said configuration memory device (23) is directly connected to said external pins (29) for program and

erase commands and configuration data to be stored in said configuration memory device; and

said security bit (24) has a second state in which only an erase command can be communicated via said external pins (29) to said configuration memory device (23) and in which said data transfer connection (27) is enabled.

Claim 1 of the appellant's auxiliary request differs from claim 1 of the main request in that the word "chip" is added in line 23 of the claim 1 filed by the appellant with the statement of grounds of appeal, so that it reads "said security bit (24) has a second state in which only a chip erase command can be communicated....".

VII. The appellant's written submissions relevant to the present decision may be summarised as follows:

In claim 1 filed with the statement of grounds of appeal, the term "directly" had been included to clearly point out that there was a direct connection between the external pins 29 and the configuration memory 23. This direct connection was not only disclosed in Figure 2 of the application by the double arrow between the configuration memory device 23 and the external pins of the multi-chip module 25, but also on page 3, lines 28 to 32 of the description. According to page 4, lines 7 to 10, the internal connection 27 was additionally provided, i. e. in addition to the connection between the configuration memory device 23 and the external pins. From this disclosure context there could be no doubt for the skilled person that the

configuration memory device 23 was directly connected to external pins 29.

Furthermore, it had been specified that in the second state of the security bit the only commands to be communicated via the external pins 29 to the configuration memory device 23 was an erase command as disclosed on page 4, lines 1 to 3 in combination with the original claim 1.

Reasons for the Decision

1. The appeal is admissible.

2.1 Claim 1 of the main request differs from claim 1 referred to in the contested decision, in that

(a) the configuration memory is "*directly*" connected to the external pins 29;

(b) only an erase command can be communicated via the external pins (29) "*to said configuration memory device (23)*" when the security bit 24 in a second state.

The fact that the configuration memory is directly connected to the external pins implies that the erase command, which is communicated via the external pins, must be communicated directly to the configuration memory device (23).

2.2 The present application does not explicitly disclose that the configuration memory 23 is directly connected

to the external pins and, in particular that an erase command can be communicated via the external pins 29 directly to the configuration memory device 23.

Thus, an essential question to be considered in the present appeal is whether the person skilled in the art could directly and unambiguously derive the combination of features a) and b) from the application as originally filed.

3.1 The double arrow shown in Figure 1 indicates that a two-way communication may be established between the external pins and the chip 23. However, in the opinion of the Board, it does not necessarily imply that this communication should take place by means of a direct connection between the pins and the chip. In fact, Figure 2 is only a schematic representation of a multichip module in a single package and does not show the actual electrical connections between the chip 23 and the external pins.

3.2 The connections between the pins and the chips 21 and 23 are specified in the description, page 3, lines 28 to 32, as follows:

- "*The external pins 29 connect to the chips 21 and 23 and an internal data connection 27 connects the configuration memory chip 23 to the logic chip 21 in a manner that permits configuration to be loaded into the logic chip 21 on power up*".

As to feature (b), it is recited in claim 1 as originally filed that "*the configuration memory*" is "*in communication with said external pins for program and*

erase commands and configuration data to be stored in said configuration memory chip" and that the security bit has a "*second state in which only an erase command can be communicated via said external pins*".

From the cited passages a person skilled in the art could only infer that there is a communication link between the external pins 29 and the configuration memory 23, and that this link is used for program and erase commands.

3.3 Hence, the Board finds no suggestion in the application documents as originally filed of a direct connection between the configuration memory device 23 and the external pins 29, as recited in claim 1 of the appellant's main request, or, in particular, of an erase command being communicated to the configuration memory device via external pins directly connected to the device.

4.1 As the amended claim 1 of the appellant's main request contains subject-matter which extends beyond the content of the application as filed, it does not comply with Article 123 (2) EPC.

4.2 Claim 1 according to the appellant's auxiliary request includes all the features of claim 1 of the main request and, therefore, comprises also subject-matter which was not disclosed in the original application.

5. As none of the appellant's requests is allowable, the present application has to be refused.

Order

For these reasons it is decided that:

The appeal is dismissed.

The Registrar: The Chairman:

U. Bultmann M. Ruggiu