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Datasheet for the decision of 4 September 2008

Case Number: T 0370/06 - 3.4.03

Application Number: 96926943.0

Publication Number: 0792513

IPC: H01L 21/033

Language of the proceedings: EN

Title of invention:
Damascene process for reduced feature size

Applicant:
ADVANCED MICRO DEVICES, INC.

Opponent:
-

Headword:
-

Relevant legal provisions:
-

Relevant legal provisions (EPC 1973):
EPC Art. 56

Keyword:
"Inventive step (no)"

Decisions cited:
-

Catchword:
-

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Case Number: T 0370/06 **-** 3.4.03

D E C I S I O N
of the Technical Board of Appeal 3.4.03
of 4 September 2008

Appellant: ADVANCED MICRO DEVICES, INC.
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Decision under appeal: **Decision of the Examining Division of the European Patent Office posted 25 January 2006 refusing European application No. 96926943.0 pursuant to Article 97(1) EPC.**

Composition of the Board:

Chairman: V. L. P. Frank
Members: G. Eliasson
J. Van Moer

Summary of Facts and Submissions

I. This is an appeal against the refusal of application 96 926 943 for lack of inventive step.

In the decision under appeal, the following prior art documents among others were cited:

D3: US 5 342 808 A; and
D5: IBM Technical Disclosure Bulletin, vol. 32, No. 1B march 1990, pages 114 and 115.

II. In a communication accompanying summons to oral proceedings, the board was of the provisional opinion that the claimed subject matter lacked an inventive step in view of documents D5 and D3. The appellant applicant responded by providing further arguments in support of inventive step and declaring that they would not attend the oral proceedings.

III. Oral proceedings were held in absence of the appellant applicant who requested in writing that the decision under appeal be set aside and a patent granted on the basis of amended claims 1 to 34 sent with the statement of grounds of appeal.

IV. Independent claim 1 reads as follows:

"1. A semiconductor device comprising:
a first dielectric material forming a layer (10), the material having a low dielectric constant, the layer having a trench (11), formation of the trench including conventional photolithography and etching techniques resulting in a trench extending

through the layer from an upper surface to a lower surface thereof, the trench being filled with conductive material to form a substantially horizontal conductive line of a conductive pattern in the layer,
characterised in that
the trench (11) has a first dimension (21) defined by a first sidewall (20) having a finite thickness (22) and comprising a second dielectric material (14) different from the first dielectric material, the second dielectric material having a hardness, density, or resistance to moisture penetration greater than that of the first dielectric material, and the conductive line being sandwiched by the second dielectric material, the thickness (22) of the sidewall (20) being such as to provide for the said first dimension (21) circumventing the limitations in the achieved dimensions of conventional photolithographic and/or etching techniques."

V. The appellant applicant's arguments can be summarized as follows:

(a) The present invention advantageously enabled flexibility in selecting the first dielectric material based on a specific property and compensating for any shortcomings by an appropriate second dielectric material. Hence there was a technical interdependence between the acknowledged two differences between the present claims and document D5 so that a separate treatment of these features was not justified.

(b) Document D5 was silent regarding the need to form, or the possibility of forming, features smaller in size than those achievable by conventional photolithographic and etching techniques, as the main objective of document D5 appeared to be the formation of a polish stop/barrier layer. Furthermore, the design rule for semiconductor devices produced at the time document D5 was published could be considered crude compared with the design rule of less than 0.3 µm targeted by the present invention.

(c) Although document D3 was the only cited document which showed the dimensions of an aperture controlled by deposition of dielectric sidewalls, it was conspicuously confined to vias and, at the time of document D3, damascene techniques involving trenches were not yet implemented in semiconductor fabrication, nor was the use of various low dielectric constant materials. Unlike vias, trenches extend horizontally and, when filled with a metal, formed a series of conductive (interconnects) which affected various performance criteria, such as circuit speed. Such conductive patterns were vulnerable to various problems not common to vias. For example, in forming conductive interconnects, electro migration and capacitance issues arose which limited circuit speed. Critical planarity issues arose in forming and filling trenches, which were not of concern in forming vias. Interconnect issues became particularly acute when employing low dielectric constant materials, particularly porous dielectric materials. Thus, the skilled person would not have

realistically led to cavalierly apply the teachings of document D3 to the formation and filling of trenches in designing circuitry.

Reasons for the Decision

1. The appeal is admissible.

2. *Inventive step*

2.1 The board considers document D5 to represent the closest prior art. It discloses the formation of interlevel metallization of a semiconductor device using dual damascene technology, ie the simultaneous creation of the trench, for the metal lead and via, for connecting lower leads, before depositing the conductive layer in the intra metal dielectric and the interlevel dielectric. The interlevel metallization is produced by forming a layer 10, 16 made of polyimide (first dielectric layer) having a trench extending through the layer (Figures 1 and 2 with accompanying description). The trench is formed using photolithography and oxygen reactive ion etching, ie conventional techniques, and is subsequently filled by a Cu or Al/Cu layer forming conductive lines and interlevel vias. The trench further has a sidewall 20 made of eg SiBN, SiON, SiN or diamond-like carbon (DLC) (second dielectric layer) which is harder than polyimide and protects the polyimide from copper diffusion. The conductive line is thus sandwiched by the sidewalls in the trench. As a consequence, the width of the trench is smaller than that achieved when the trench was etched in the polyimide layer.

2.2 The device of claim 1 differs from that of document D5 in that (i) the first dielectric material has a low dielectric constant, whereas in document D5 polyimide is used which is not regarded as a "low-κ" material; and (ii) the thickness of the sidewall is chosen so as to circumvent the limitations in the achieved dimensions of conventional photolithographic and/or etching techniques.

2.3 Both features (i) and (ii) have the technical effect of allowing the feature sizes of a semiconductor device to shrink but in different aspects: Feature (i) enables a reduction of the distance between adjacent interconnection lines due to the reduced electromagnetic coupling between adjacent interconnection lines, whereas feature (ii) makes it possible to shrink the dimensions of the interconnection lines and vias themselves. Thus, although features (i) and (ii) both relate to reduced feature sizes, they relate to different aspects of this technical aim.

2.4 The appellant applicant argued in this context that there was a technical interdependence between features (i) and (ii) so that these features could not be treated separately in the assessment of inventive step (see item V(a) above). The board is not persuaded by this argument, since such a technical interdependence between features (i) and (ii) would have to manifest itself either in form of a synergy effect from the combination of measures (i) and (ii) or in form of a dependence of one of features (i) and (ii) on the other in order to perform its intended function. The board is

not able to find this kind of interdependence alleged by the appellant applicant. Therefore, features (i) and (ii) can be treated separately in the assessment of inventive step.

2.5 Regarding feature (i), a skilled person faced with the problem of reducing the distance between adjacent interconnection lines in the device of document D5 would in the board's opinion routinely consider using so-called "low-κ" materials having a low dielectric constant instead of polyimide, in particular since the device of document D5 already has sidewalls 20 and etch stop layers 14, 18 which would provide the necessary protection of the "low-κ" dielectric material from the environment.

2.6 As to feature (ii), the board agrees with the examining division that the use of sidewalls in trenches was at the priority date of the application a well-known means for reducing the horizontal dimension of a trench beyond that attainable by conventional lithography and etching techniques. In particular, document D3 discloses the use of sidewalls for this purpose in a via trench to be filled with metal (see column 1, lines 58 to 63 and Figures 1A to 1C with accompanying text). A skilled person faced with the task of reducing the dimensions of vias and interconnection lines of the device of document D5 beyond that attainable using conventional lithography would therefore consider using the teaching of document D3 to set the thickness of the sidewalls accordingly.

2.7 Appellant applicant argued that document D5 was concerned with the formation of a polish stop/barrier

layer in a semiconductor device having much larger dimensions than that attained by the present invention (see item V(b) above). The board does not dispute that at the time document D5 was published (in March 1990), the typical feature size of semiconductor devices was considerably larger than that attainable at the priority date of the present application (September 1995), a fact that the skilled person when reading document D5 at the priority date would certainly be aware of. Hence the skilled person knowing the continuous improvement in semiconductor manufacturing technology since the publication of document D5 would realise that this process would also be capable of producing smaller feature sizes than those available at its publication date.

2.8 The argument by the appellant applicant that document D3 was confined to vias and not interconnection lines fails to convince the board, since the dimensional problems become particularly acute for vias having higher aspect ratio than a trench defining an interconnection line (see item V(c) above). The particular issues mentioned for interconnection lines, such as electro migration and capacitance issues, are not related to the question whether or not the skilled person would consider the use of sidewalls for limiting the width of a trench. It should also be kept in mind that the use of sidewalls for lining trenches defining interconnection lines is already known from document D5.

2.9 For the above reasons, in the board's judgement, the subject matter of claim 1 lacks an inventive step within the meaning of Article 56 EPC 1973.

Order

For these reasons it is decided that:

The appeal is dismissed.

Registrar Chair

G. Rauh V. L. P. Frank