BESCHWERDEKAMMERN DES EUROPÄISCHEN PATENTAMTS

BOARDS OF APPEAL OF THE EUROPEAN PATENT OFFICE

CHAMBRES DE RECOURS DE L'OFFICE EUROPEEN DES BREVETS

Internal distribution code:
(A) [ ] Publication in OJ
(B) [ ] To Chairmen and Members
(C) [ ] To Chairmen
(D) [X] No distribution

Datasheet for the decision of 29 April 2008

Case Number: T 0352/06 - 3.5.02

Application Number: 00984487.9

Publication Number: 1243073

IPC: H03K 19/003

Language of the proceedings: EN

Title of invention:
Circuitry and method for removing glitches in digital circuits

Applicant:
HONEYWELL INC.

Headword:
-

Relevant legal provisions:
EPC Art. 54

Relevant legal provisions (EPC 1973):
-

Keyword:
"Novelty - no"

Decisions cited:
-

Catchword:
-

Europäisches Patentamt | European Patent Office | Office européen des brevets

Beschwerdekammern | Boards of Appeal | Chambres de recours

Case Number: T 0352/06 - 3.5.02

D E C I S I O N
of the Technical Board of Appeal 3.5.02
of 29 April 2008

Appellant: HONEYWELL INC.
101 Columbia Avenue
P.O. Box 2245
Morristown, NJ 07960 (US)

Representative: Haley, Stephen
Gill Jennings & Every LLP
Broadgate House
7 Eldon Street
London EC2M 7LH (GB)

Decision under appeal: **Decision of the Examining Division of the European Patent Office posted 9 November 2005 refusing European application No. 00984487.9 pursuant to Article 97(1) EPC.**

Composition of the Board:

Chairman: M. Ruggiu
Members: M. Rognoni
E. Lachacinski

Summary of Facts and Submissions

I. The appellant (applicant) appealed against the decision of the examining division refusing European patent application No. 00 984 487.9.

II. In the decision under appeal, the examining division held, *inter alia*, that the subject-matter of claim 1 then on file lacked novelty with respect to the following document:

D1: EP-A-0 264 614.

III. Oral proceedings before the Board were held on 29 April 2008.

V. The appellant requested that the decision under appeal be set aside and that a patent be granted on the basis of claims 1 to 6 filed with a letter dated 22 February 2006.

VI. Claim 1 of the appellant's request, which is the same as the independent claim considered in the contested decision, reads as follows:

"A digital circuit having an input and comprising:
a p-channel;
an n-channel;
a negative glitch suppressor coupled between the input and the p-channel but not to the n-channel; and
a positive glitch suppressor coupled between the input and the n-channel but not to the p-channel."

Claims 2 to 6 are dependent on claim 1.

VII. The appellant's arguments relevant to the present decision may be summarised as follows:

The present application solved the problem of reducing or eliminating unwanted signal glitches from electronic data transmission and processing systems by providing a circuit, as specified in claim 1, which removed negative glitches from the input to a p-channel transistor and positive glitches from the input to an n-channel transistor.

Document D1 disclosed a MOSFET drive circuit providing protection against transient voltage breakdown. The circuit was designed to produce a high voltage output signal in response to a low input voltage. With reference to Figure 7 of D1, a "crow-bar current" arose when, for a short period of time, both the p-channel transistor 4 and the n-channel transistor 5 were "on" and a short circuit was created between V_H and V_L. D1 sought to reduce the "crow-bar current" produced during switching of the transistors 4 and 5 by providing a drive circuit which separated an input signal into a first signal (the branch containing inverter 11) and a second signal (the branch containing buffer 16). The first signal was processed in order to delay any rising edges of the input signal by a specific time period before passing it to the p-channel transistor 4 (cf. D1, Figures 7 and 8). The second signal was processed in order to delay any falling edges by a specific time period before passing it to the n-channel transistor 5. In each case, the specific time period was larger than the rise time of either the p-channel transistor 4 or the n-channel transistor 5.

Because of the presence of the inverter 11, branch 11 – 15 of the circuit according to Figure 7 could only function as an inverting positive glitch suppressor, which was contrary to the wording of claim 1 which required a "negative glitch suppressor coupled between the input and the p-channel but not to the n-channel". Similarly, elements 16 - 20 of the lower branch of the circuit of Figure 7 could only function as an inverting negative glitch suppressor and not as a positive glitch suppressor as specified in claim 1 of the present application. The different functionalities provided by the circuit known from D1 clearly showed that it was not meant to provide glitch suppression according to the present invention, but was only concerned with the problem of reducing crow-bar currents in a MOSFET drive circuit.

There was in fact no suggestion in D1 that the circuits connected between the input and the transistors for the purpose of delaying the pulses which switched on the transistors should operate as glitch suppressors or that some form of glitch suppression should be provided for a digital circuit comprising a p-channel and an n-channel.

Even if there appeared to be some similarities between the circuit of Figure 7 and some of the embodiments of the present invention, the circuit known from D1 addressed a different problem and thus was meant to operate in a substantially different way. In summary, as far as glitch suppression was concerned, D1 was not an enabling disclosure and, as such, could not anticipate the present invention.

The subject-matter of claim 1 was therefore new within the meaning of Article 54 EPC.

Reasons for the decision

1. The appeal is admissible.

2.1 The present application deals, *inter alia*, with the problem of eliminating unwanted signal "glitches" in a digital circuit which comprises a p-channel and an n-channel. As pointed out in the description (application as published, page 1, lines 7 to 11), the "*signals in most digital systems have two idealized states, namely, a low voltage state and a high voltage state. Unwanted transitions of a signal from a first voltage state to another, and then back to the first is* [sic] *often referred to as a glitch.*" In other words, any unwanted positive or negative pulses shorter than the expected signal pulses can be regarded as "glitches" according to the present application.

2.2 The gist of the present invention consists essentially in "*providing a glitch removal circuit that removes negative glitches from those signals that are provided to circuit elements that are turned-on by negative glitches (e.g., p–channel transistors), and/or removes positive glitches from those signals that are provided to circuit elements that are turned on by positive glitches (e.g., n-channel transistors)*" (application as published, page 2, lines 11 to 15).

2.3 As shown in Figure 2 of the application, "a glitch suppressor" according to the present invention includes a logic block 202 and a delay line 207 connected to one of the block's two input terminals. Depending on the logic function of the logic block 202, the "*pulse suppression circuit of Figure 2 can provide a negative pulse suppression circuit, a positive pulse suppression circuit, an inverting negative pulse suppression circuit or an inverting positive pulse suppression circuit*" (application as published: page 7, lines 11 to 14).

As illustrated in Figure 3, the logic block of a positive pulse suppressor is an AND gate whose output signal level is LOW as long as one of the two input signals remains LOW. The logic block of a negative pulse suppressor is an OR gate whose output signal level is HIGH when at least one of the inputs is HIGH. As the timing chart of Figure 3 shows, input voltage transitions are delayed by the delay line 207 so that a positive pulse of short duration, *i.e.* shorter than the time delay introduced by the delay line 207, never appears simultaneously at both inputs of the AND gate 215 and thus never switches the AND gate from LOW to HIGH. Similarly, a negative pulse cannot switch the OR gate 260 from HIGH to LOW, unless its duration is greater than the delay provided by the delay line 207. In other words, a momentary transition from a high voltage state to a low voltage state, *i.e.* a "*negative glitch*", has no influence on the output of the OR gate and is therefore "*suppressed*". The same happens to "*positive glitches*" at the input 203 when the logic block corresponds to an AND gate (see Figure 2).

2.4 As specified in the description of the present application (page 3, lines 15 to 19), when applied to an inverter, the "*negative pulse suppression circuit of the present invention can be used to delay negative transitions at the gate of the p-channel transistor while not delaying positive transitions. Likewise, the positive pulse suppression circuit can be used to delay positive transitions at the gate of the n-channel transistor while not delaying negative transitions.*" This has not only the effect of suppressing negative glitches at the gate of the p-channel transistor and positive glitches at the gate of the n-channel transistor. It also turns off the "on" transistor before turning on the "off" transistor after a transition of the inverter's input signal. As a result, "crow-bar" currents from the power supply to ground "*may be significantly reduced or eliminated*" (see published application, page 3, lines 19 to 24).

Article 54 EPC

3.1 Figure 7 of D1 shows a push-pull drive circuit comprising a p-channel transistor 4, an n-channel transistor 5, a circuit branch for producing a fixed delay before a rising edge of the input signal level is applied as a falling edge of the input signal to the gate of the p-transistor and a circuit branch for producing a fixed delay before a falling edge of the input signal is applied as a rising edge of the input signal to the n-transistor gate. "*As a result, during a level transition of the input signal applied to the circuit, the timing at which the one of the P-channel MOS FET and N-channel MOS FET which was previously in the OFF state is changed to the ON state is delayed*

with respect to the timing at which the other FET is changed from the ON to the OFF state." (D1, column 11, lines 41 to 47)

It is implicit to a person skilled in the art that a transition of the input signal from a low voltage state to a high voltage state does not appear as a HIGH-to-LOW transition at the gate of the p-channel transistor 4, when its duration is shorter than the delay introduced by the buffer circuits 12 and 13. Similarly, a momentary transition of the input signal from a high voltage state to a low voltage state shorter than the delay introduced by the buffer circuits 17 and 18 does not appear as a LOW-to-HIGH transition at the gate of the n-channel transistor 5.

3.2 In other words, Figure 7 of D1 shows a digital circuit comprising a p-channel, an n-channel, a first circuit branch coupled between the input and the p-channel and a second circuit branch coupled between the input and the n-channel, whereby the first circuit branch suppresses only positive input glitches in the input signal, *i.e.* of the polarity required to switch on the p-channel transistor, and the second circuit branch suppresses only negative input glitches, *i.e.* of the polarity which switches on the n-channel transistor.

Hence, as correctly observed by the appellant, the branch 11 – 15 of the circuit according to Figure 7 functions as an inverting positive glitch suppressor, whereas the branch 16 – 20 is an inverting negative glitch suppressor.

3.3 It is, however, pointed out in D1 (column 11, lines 18 to 21) with reference to the embodiment of Figure 7 that if "*the phase of the output signal is to be inverted with respect to that of the input signal, then the inverter 11 could be replaced by a buffer, and buffer 16 replaced by an inverter.*" Furthermore, if the gate input levels of the p-channel and n-channel transistors are the same, "*then level shifters 2 and 3 can be omitted*" (D1, column 11, lines 25 and 26).

In this case the circuit branch comprising the OR gate 14 and the delay elements 12 and 13 acts as a suppressor of negative pulses whose lengths are shorter than the delay introduced by the elements 12 and 13 (cf. Figure 3 of the application, circuit 202b). On the other hand, the circuit branch comprising an OR gate 19 with an inverter 20 at the output, *i.e.* a NOR gate, delays negative pulses and converts them into positive pulses. Only negative input pulses which are longer than the delay introduced by the delay elements 17 and 18 appear at the output of the OR gate and are thus applied to the n-channel transistor. By inverting the input, the inverting negative pulse suppressing branch in the circuit of Figure 7 becomes a positive pulse suppressor, in the sense that it delays the transmission of a positive pulse from the input to the gate of the n-channel transistor and thus inevitably suppresses positive pulses which are shorter than the delay introduced by the delay elements 17 and 18.

3.4 In summary, the teaching of D1 as illustrated in Figure 7 and applied to an inverter as suggested in column 11, lines 18 to 21, results in a digital circuit having an input and comprising a p-channel, an n-

channel, a first circuit branch coupled between the input and the p-channel but not to the n-channel and a second circuit branch coupled between the input and the n-channel but not to the p-channel. As explained above, the first circuit branch delays only the transmission of negative input pulses to the p-channel transistor, and effectively suppresses unwanted negative pulses shorter than the predetermined delay period. Similarly, the second circuit branch delays only the transmission of positive pulses to the n-channel transistor and thus blocks positive pulses shorter than the predetermined delay period.

3.5 The appellant has essentially argued that D1 could not take away the novelty of the claimed subject-matter because it did not address the problem of glitch suppression. Despite the accidental similarities between the circuit of the invention and the circuit shown in Figure 7 of D1, the latter was not meant to operate as a glitch suppressor. It merely delayed the switching on of the transistor in the off-state with respect to the switching off of the transistor in the on-state.

3.6 The Board agrees with the appellant that D1 does not explicitly deal with the problem of glitch suppression in a digital circuit comprising a p-channel transistor and an n-channel transistor. However, D1 relates, *inter alia*, to an inverter output stage which comprises a first circuit branch coupled between the input and the p-channel transistor but not to the n-channel transistor and a second circuit branch coupled between the input and the n-channel but not to the p-channel transistor. As pointed out above, it is an intrinsic

functionality of the first and second circuit branches to block the transmission of negative and positive pulses, respectively, when these are shorter than the time interval corresponding to the time delay introduced by the delay elements 12 and 13 or 17 and 18. Furthermore, this functionality is not dependent on any particular choice of circuit components and, though not explicitly mentioned in D1, is revealed by an elementary analysis of the circuit within the reach of any skilled person.

3.7 In the result the Board finds that D1 discloses a circuit which comprises all features recited in claim 1 of the appellant's request. The subject-matter of this claim is therefore not novel within the meaning of Article 54 EPC.

4. As the appellant's only request does not provide a basis for an allowable claim, the application has to be refused.

Order

For these reasons it is decided that:

The appeal is dismissed.

The registrar: The Chairman:

U. Bultmann M. Ruggiu