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Datasheet for the decision of 12 February 2010

Case Number: T 0342/06 - 3.4.03

Application Number: 96307374.7

Publication Number: 0798689

IPC: G09G 1/16

Language of the proceedings: EN

Title of invention:
Display processor system for bit-mapped displays of waveform data

Patentee:
FLUKE CORPORATION

Opponent:
-

Headword:
-

Relevant legal provisions:
EPC Art. 123(2)
EPC R. 103(1)(a)

Relevant legal provisions (EPC 1973):
EPC Art. 54, 56

Keyword:
"Novelty (yes)"
"Inventive step (yes)"
"Reimbursement of appeal fee (no)"

Decisions cited:
-

Catchword:
-

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Case Number: T 0342/06 - 3.4.03

D E C I S I O N
of the Technical Board of Appeal 3.4.03
of 12 February 2010

Appellant: FLUKE CORPORATION
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Decision under appeal: **Decision of the Examining Division of the European Patent Office posted 15 September 2005 refusing European patent application No. 96307374.7 pursuant to Article 97(1) EPC 1973.**

Composition of the Board:

Chairman: G. Eliasson
Members: E. Wolff
J. Van Moer

Summary of Facts and Submissions

I. The examining division refused European patent application No. 96307374.7 for lack of novelty.

II. The examining division relied in its decision on prior art document

D1 = EP 0 261 256 A.

III. The appellant requested that the decision of the examining division be set aside and the patent be granted on the basis of the new main request filed during oral proceedings. The appellant further requested that the appeal fee be reimbursed.

IV. The independent claims 1 and 5 of the main request read as follows:

1. A method for producing desired display images on a bitmapped display (12) by combining selected ones of a set of bit plane images stored in a display memory (28), said set of bit plane images comprising a plurality of predetermined images for building said desired display images,

the method being characterised by the steps of, for each desired image:

(a) establishing a display operation sequence, by defining a selected set of bit plane images from said set of bit plane images, how each bit plane image is operated on and applied to a display image, by selecting from a set of a plurality of

display operations, and the order in which the bit plane images are retrieved, operated on and applied to the display image;

(b) employing the display operation sequence by operating on a display image, retrieving each of said selected bit plane images in sequence, employing each of said bit plane images and each respective operation in sequence, according to the display operation sequence, to obtain the respective desired display image; and

(c) displaying said desired display image on said bit-mapped display(12), wherein the display image is continuously rebuilt as successive frames, each frame according to the display operation sequence.

5. A display processing system for providing desired display images, the system comprising:

(a) a display memory (28) for storing a set of bit plane images;

(b) means (24) for defining a display operation sequence, including a selection of a set of bit plane images, how each bit plane image is operated on and applied to a display image, by selecting from a set of a plurality of display operations, and the order in which the bit plane images are retrieved, operated on and applied to the display image;

(c) an accumulator coupled to selectively receive bit plane image data from said display memory (28) and

to operate on a display image using said selected bit plane images sequentially according to said display operation sequence, in order to build a desired display image; and

(d) a bit-mapped display (12) coupled to said accumulator to receive and visually display said desired display image, wherein the display image is continuously rebuilt as successive frames, each frame according to the display operation sequence.

V. The arguments made by the appellant can be summarised as follows:

The independent claims of the request recited that the selected bit plane images were stacked on top of one another according to the display operation sequence, that the order in which the operations occurred according to the display operation sequence determine what the displayed image looks like, and that the display image was continuously rebuilt as successive frames, with each frame being built according to the display operation sequence.

These features emphasised the differences between the present invention and the disclosure in document D1 and made clear that the invention did not employ the conventional serial processing of groups of pixels as disclosed in document D1, where serial bit streams representing pixel planes were operated on simultaneously (in parallel).

As regards the request for the refund of the appeal fee, the appellant argued that that the decision of the

examining division was not adequately reasoned and that therefore a substantial procedural violation had occurred.

Reasons for the decision

1. Admissibility

The appeal is admissible.

2. Request for refund of the appeal fee

2.1 A request of a refund of the appeal fee is justified in cases where a substantial procedural violation has occurred (Rule 103(1)(a) EPC (Rule 67 EPC 1973)).

2.2 The examining division has provided a detailed analysis of the claimed features (apparatus and method) and how they relate to those found in the prior art. They arrived at their conclusion on the basis of this analysis. Their analysis may possibly turn out to be incorrect, but cannot for that reason be said to be inadequate.

2.3 The board concludes that contrary to the appellant's allegations, the examining division had provided a reasoned decision and that therefore no substantial procedural violation has occurred. The request for reimbursement of the appeal fee is therefore refused.

3. Amendments

3.1 Claims 1 and 5 of the request differ from the corresponding claims before the examining division by the addition in each claim at the end of the last paragraph of the wording "wherein the display image is continuously rebuilt as successive frames, each frame according to the display operation sequence".

3.2 The basis for this amendment is to be found verbatim in column 3, lines 38 to 41 of the published application. Although mentioned in the specific context of explaining how a menu box previously inserted into the display image is subsequently removed again, the board is satisfied that continuous rebuilding of the image as successive frames, each frame in accordance with the display operation sequence, is a feature generally applicable to the claimed method.

3.3 The board is satisfied that this amendment conforms with the requirements of Article 123(2) EPC.

4. Novelty (Art. 54 EPC 1973)

4.1 Document D1 constitutes the nearest prior art. It relates to a display controller for cathode ray tube (CRT) displays. The controller employs what is referred to in document D1 as "video objects". These video objects are graphic elements, graphs or alphanumeric characters which cover some or all of the screen. The video objects are stored in a video information storage medium. When generating the video output signal, the video objects relevant for the relevant area of the

screen are read out in parallel and their signals combined to form the video output signal.

4.2 More specifically, in one form of carrying out the method of document D1, the output of each RAM page (7a, 7b, 7c) is supplied to an associated shift register, with each shift register providing a serial bit stream output (see Fig. 2 and its accompanying description). These serial bit streams are then simultaneously clocked out of the shift registers belonging to the various RAM pages. N signals thus generated from N video objects or, more precisely, the RAM pages belonging to those N objects, are transmitted in parallel to a combination logic (11), where they are combined under the control of a control input (an enable signal) into the video output which usually is a single video output signal (13), although generation of a plurality of video output signals is also envisaged in passing (column 3 line 45 to column 4, line 5). The combination logic consists, for example, of AND gates or NAND gates (18a to 18c and 36a to 36c in Figures 3 and 4, respectively) which combine the serial bit streams corresponding to the parallel video objects into a video output signal. There is also a brief mention of another possible configuration in which the non-serialised data are first processed in the combination logic, and serialisation is performed subsequent to the signals having passed the combination logic (column 4, lines 5 to 8).

4.3 Irrespective of whether the signals representing the different video objects are first serialised and then combined or combined first and then serialised, what all display operations disclosed in document D1 have in

common is that the video output signal is the result of combining into a single signal the signals from different pixel planes representing the different video objects. To this end, the signals from different video objects or pixel planes are synchronously clocked and supplied in parallel to the combination logic where they are combined into the video output signal, or as is peripherally mentioned (column 3 line 45 to column 4, line 5) more than one video output signal.

4.4 The invention as claimed employs bit planes which resemble the pixel planes or video objects of document D1 and contain preset images such as grid lines, coordinate axes, labels and the like. In addition, a set of display operations such as SET, NOP (= no operation), MASK, or INVERT are defined which determine whether and if so how each of a selected set of bit planes interacts with the display image. For example, the display operation SET acting on a bit plane containing gridlines will impose those gridlines on the display image, with a subsequent change of the display operation for this bit plane to NOP making those grid lines disappear again by turning the corresponding bit plane off (application, column 3, lines 1 to 3 and lines 32 to 37; and column 11, lines 29 to 32).

4.5 To build a complete frame of the display image, a display operation sequence is used which specifies both the set of bit planes images to be used and the display operation to be performed on a given bit plane (Column 8, lines 4 to 9). Each frame of the display is built according to its display operation sequence, the display itself being continuously rebuilt as successive frames.

4.6 The claimed invention thus differs from the display technique disclosed in document D1 in that the display is not formed by simultaneously combining for each pixel the different video objects from all relevant pixel planes as in document D1, but, instead, building the display image by applying a succession of bit planes to the display image in the manner determined by the associated display operation and then continuously rebuilding the display as successive frames, with each frame being built in accordance with the display operation sequence set for it. Since independent method claim 1 specifies these steps, and the apparatus claim 5 specifies apparatus features needed to carry out this method, the invention as claimed in both independent claims is novel over the disclosure in document D1.

4.7 The claimed invention is novel also with respect to a method of forming a display which is discussed as relevant prior art in document D1. That method builds a display line by line and requires that a video controller, in order to place various objects at their correct position on the screen, must continuously look up an object description table. The look-up is performed on a line-by-line basis in that for each line on the video screen the video controller performs a check in the object description table for any and all objects which affect that line (document D1, Figure 1 and column 7, lines 3 to 10).

5. Inventive step

5.1 According to the application, the distinguishing features make minimal the burden on the microprocessor of building and then rebuilding a display image (column 4, lines 25 to 37).

5.2 Hence, the problem addressed by the claimed invention is to reduce the processing burden on the microprocessor when building a display image in a measuring instrument.

5.3 There is no indication in the cited prior art which would lead the skilled person from the disclosed known techniques of forming the display to building the display image by defining a display operation sequence which defines a set of bit planes required for building the display together with the sequence of display operations to be applied to them.

5.4 The board therefore concludes that the claimed invention involves an inventive step as required by Article 56 EPC 1973.

Order

For these reasons it is decided that:

1. The decision under appeal is set aside.

2. The case is remitted to the first instance with the order to grant a patent with the following documents:

   (a) claims 1 to 8 (request submitted at the oral proceedings);

   (b) description: pages 1 to 3, 3a, 7, 10, 12-16 filed with letter dated 30 April 2002, pages 4-6, 8, 9, 11, 17 as originally filed;

   (c) 1-6 and 8 as originally filed, 7 filed with letter of 30 April 2002.

3. The request for reimbursement of the appeal fee is refused.

Registrar Chair

S. Sánchez Chiquero G. Eliasson