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**Datasheet for the decision
of 24 September 2009**

Case Number: T 0294/06 - 3.4.03

Application Number: 98902263.7

Publication Number: 0895219

IPC: G09G 3/30

Language of the proceedings: EN

Title of invention:

Display device

Applicant:

Seiko Epson Corporation

Opponent:

-

Headword:

-

Relevant legal provisions:

EPC Art. 123(2)

Relevant legal provisions (EPC 1973):

EPC Art. 56

Keyword:

"Inventive step - (yes) after amendment"

Decisions cited:

-

Catchword:

-



Case Number: T 0294/06 - 3.4.03

D E C I S I O N
of the Technical Board of Appeal 3.4.03
of 24 September 2009

Appellant:

Seiko Epson Corporation
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Representative:

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Decision under appeal:

Decision of the Examining Division of the
European Patent Office posted 25 July 2005
refusing European application No. 98902263.7
pursuant to Article 97(1) EPC.

Composition of the Board:

Chairman: G. Eliasson
Members: E. Wolff
T. Bokor

Summary of Facts and Submissions

I. This is an appeal against the decision of the examining division to refuse European patent application No. 98 902 263.

II. In its decision, the examining the division cited the following documents, among others:

D1: EP 0 653 741 A

D3: LEWIS A G; LEE D D; BRUCE R H "POLYSILICON TFT CIRCUIT DESIGN AND PERFORMANCE" IEEE JOURNAL OF SOLID-STATE CIRCUITS, IEEE INC. NEW YORK, USA, VOL. 27, NR. 12, 01.12.1992, pg. 1833-1842

The patent application was refused on the ground that the subject matter of claim 1 of the request before the examining division did not involve an inventive step over document D1 and general knowledge in the field of electronics.

III. At the appeal stage the appellant filed a further document

D5: US 5 844 534 A

in support of the appellant's arguments concerning the gate voltages applied in prior art circuits.

IV. At oral proceedings before the board, the appellant requested that the decision under appeal be set aside and a patent granted on the basis of

Specification: pages 1-68 filed during oral proceedings.
Claims: 1 to 10 filed during oral proceedings.
Drawings: Sheets 1-31 as originally filed.

V. Claim 1 of the above request reads as follows:

"1. *A display apparatus comprising:*

a plurality of scanning lines;

a plurality of data lines intersecting said plurality of scanning lines;

a plurality of power supply lines; and

a plurality of pixels disposed corresponding to intersections of said scanning lines and said data lines in a matrix, each of said pixels including

a first thin film transistor (20) having a first gate electrode connected to one of said plurality of scanning lines,

a holding capacitor arranged to hold a signal supplied through one of said plurality of data lines via said first transistor (20),

a second thin film transistor (30) having a second gate electrode connected to the holding capacitor; and

a luminescent element (40) provided between a pixel electrode (41) corresponding to each of said

pixels and an opposite electrode opposed to said pixels, each of said pixel electrodes being able to be electrically connected to a said power supply line, characterised in that:

the first transistor (20) is provided between the said data line and the second gate electrode, the second transistor (30) is provided between a said power supply line (com) and the pixel electrode (41), the luminescent element being able to emit light due to driving current that flows between said pixel electrode (41) and said opposite electrode when said pixel electrode (41) is electrically connected to the said power supply line through said second transistor (30),

said second transistor is of P channel type and a potential of said power supply line is arranged to be set at a higher level than that of said opposite electrode, and the potential of the gate electrode of said second transistor when said pixel electrode is electrically connected to said power supply line is arranged to be higher than the potential of the opposite electrode and lower than the potential of said power supply line."

VI. The arguments presented by the appellant in favour of the request can be summarised as follows.

The electroluminescent display disclosed in the nearest prior art document, D1, offers no information about the voltage regime of the pixel drive circuit. Document D3 served to illustrate the general understanding of the skilled person at the time the invention was made,

which was that in order to minimise the resistance of the transistor switching the electroluminescent device it was necessary to employ a high gate voltage, well in excess of the drain bias. This was the normal practice in the art at the priority date of the invention. In contrast, the present invention was based on the then counter-intuitive idea that a moderate increase in the drain bias of the thin-film transistor that switches the electroluminescent display permitted a significant reduction of the gate voltage, thereby making the circuit overall more energy efficient.

Reasons for the decision

1. *Admissibility*

The appeal is admissible.

2. *Amendments*

2.1 Claim 1 is based on claims 2 and 4 together with the embodiments of figures 17 to 20 of the application as filed and has been amended for clarity.

2.2 The description was amended to match the ambit of the sole remaining independent claim 1. This was achieved by removing from the description references to embodiments no longer covered by the wording of the claim.

2.3 The board is satisfied that the claims and the amended description do not introduce any subject-matter going beyond the contents of the application as filed and

therefore comply with the requirements of Article 123(2) EPC.

3. *Novelty and inventive step*

3.1 It is common ground that document D1 constitutes the closest prior art and that the invention as claimed in claim 1 of the main request is new over the disclosure in that document.

3.2 Document D1 discloses in Figure 2 (itself acknowledged prior art with respect to the invention to which document D1 relates) a pixel element of an electroluminescent display, the drive circuit of which has the same overall configuration of circuit elements as the circuit of the claimed invention, with the exception that the thin film transistors (TFTs) in Figure 2 of document D1 are N-channel type TFTs.

3.3 There are only two voltages explicitly referred to in document D1. One is in respect of a simple matrix type electro-luminescent panel (Fig. 1) without any memory function, for which the pulse driving voltage is 20V to 30V, with the luminance being a function of the pulse width. The other mention occurs in relation to Figure 3 which describes a first embodiment of the invention to which document D1 relates. That embodiment shares with the invention the feature that a memory capacitor is connected to the gate of the TFT which is connected in series with the electro-luminescent device and which controls the current flow through it. The only other voltage mentioned in document D1 is drive voltage of the electro-luminescent device which is stated to be about 7V. No other operating voltages are disclosed.

Therefore, in order to assess whether it is indeed a distinguishing feature of the claimed invention that the potential of the gate electrode is at a potential intermediate the potentials applied to the power supply line and the opposite electrode, it needs to be established what were the operating voltages that were employed in the prior art circuits.

3.4 The appellant argued that the function of a typical prior art circuit was fully explained in the application with respect to Figures 31 to 33.

3.4.1 In this prior art circuit, as well as in the circuits described in document D1, the low resistance of the current path through the TFT connected in series with the electro-luminescent device was achieved by the conventional means of applying a high gate voltage, as shown in particular in Figure 33 of the application. In document D1 this applied not only to the circuit described there as being itself prior art but also to circuits according to the invention of document D1.

3.4.2 This modus operandi of the prior art circuits was confirmed by the disclosure in document D3. Document D3 showed, in particular with reference to its Figure 2, that with a gate voltage $V_{GS}=6V$ a variation of the drain voltage V_D over a wide range, from below about 2V to 15 V, had little influence on the drain current. This applied to both N-channel TFTs and (Figure 2a) and P-channel TFTs (Figure 2b).

3.4.3 That same Figure 2 of document D3 would suggest to the skilled person seeking to lower the resistance of the TFT that the gate voltage V_{GS} would need to be increased.

Document D3 further stated explicitly that the voltage swing needed on the gate lines was around 15V, compared to a drain bias of about 5V (page 1834, left-hand column, lines 31 to 36; page 1836, left-hand column, lines 1 and 2; Figure 4).

- 3.4.4 Of the remaining documents, only document D5 discloses the voltages to be applied to particular TFT circuit configurations. It discloses a voltage swing on the gate lines of 40 V or more (cf. column 11, lines 13 to 16 and 46 to 53; column 12, lines 44 to 50).
- 3.5 On the basis of what the cited prior art documents disclose, the board accepts the argument that the prior art circuits including the circuits in document D1 employed a high gate voltage to reduce the internal resistance of the switching TFT for the luminescent device.
- 3.6 Therefore, taking document D1 as the nearest prior art, the differences which distinguish the invention as claimed in claim 1 are the use of a P-channel TFT as the switching transistor connected in series with the luminescent device, and the different relative magnitudes of the potentials applied to the circuit.
- 3.7 In the light of these differences, the objective problem to be solved by the invention is to improve an electroluminescent display device by improving the characteristics of the circuit driving the luminescent device. The claimed invention achieves that goal by using a P-channel TFT and the claimed relationship between the potential of said power supply line the

opposite electrode, with the potential of the gate electrode having to lie between the other two.

3.8 The solution allows the gate voltage to be reduced significantly. There is no indication in any of the prior art documents that the objective problem was amenable to solution by the claimed features. The solution is based on the appreciation that a relatively small increase in the drain bias V_D permits a significant reduction in the gate voltage V_{GS} . More specifically, the potential of the gate electrode of said second thin film transistor when said pixel electrode is electrically connected to the power supply line is arranged to be higher than the potential of the opposite electrode and lower than the potential of said power supply line.

3.9 In response to the objection raised by the board in its communication which accompanied the summons to oral proceedings, which was that the skilled person would have understood from Figures 2a) and 2b) of document D3 that the gate voltage could be reduced by increasing the drain bias, the appellant argued convincingly that while, admittedly, the skilled person could have arrived at the principle of the present invention, Document D3 provided no incentive to depart from the conventional manner of reducing the resistance of the TFT by increasing the gate voltage. Therefore, the skilled person would not have considered that document D3 suggested the solution provided by the present invention.

3.10 For the reasons set out above, the board considers that the invention as claimed in claim 1 involves an inventive step as required by Article 56 EPC 1973.

Order

For these reasons it is decided that:

1. The decision under appeal is set aside.
2. The case is remitted to the department of first instance with the order to grant a patent on the basis of the following documents:

Specification: pages 1-68 filed during oral proceedings.

Claims: 1 to 10 filed during oral proceedings.

Drawings: Sheets 1-31 as originally filed

Registrar

Chair

S. Sánchez Chiquero

G. Eliasson