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Datasheet for the decision of 19 September 2008

Case Number: T 0217/06 - 3.4.03

Application Number: 94307556.4

Publication Number: 0650197

IPC: H01L 27/12

Language of the proceedings: EN

Title of invention:
Thin film semiconductor integrated circuit and method of fabricating the same

Applicant:
SEMICONDUCTOR ENERGY LABORATORY CO., LTD

Opponent:
-

Headword:
-

Relevant legal provisions:
EPC Art. 123(2)

Relevant legal provisions (EPC 1973):
EPC Art. 56

Keyword:
"Inventive step - main request (no)"
"Added subject-matter - auxiliary request (yes)"

Decisions cited:
-

Catchword:
-

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Case Number: T 0217/06 - 3.4.03

D E C I S I O N
of the Technical Board of Appeal 3.4.03
of 19 September 2008

Appellant: SEMICONDUCTOR ENERGY LABORATORY CO., LTD.
398 Hase
Atsugi-shi, Kanagawa-ken 243-0036 (JP)

Representative: Rummler, Felix
R.G.C. Jenkins & Co
26 Caxton Street
London SW1H 0RJ (GB)

Decision under appeal: **Decision of the Examining Division of the European Patent Office posted 16 August 2005 refusing European application No. 94307556.4 pursuant to Article 97(1) EPC.**

Composition of the Board:

Chairman: G. Eliasson
Members: E. Wolff
J. Van Moer

Summary of Facts and Submissions

I. This is an appeal against the decision of the examining division to refuse European patent application 94 307 556.4.

II. The application was refused under Articles 97(1) and 113(2) EPC 1973 because none of the amended requests complied with Article 123(2) EPC 1973, the examining division having exercised its discretion not to admit those amendments. Yet, the examining division also indicated that an amendment which would limit the claims to the embodiment of Figures 5A to E might be acceptable.

III. The following prior art documents, among others, were cited during examination

D4: CN-107.00.52 together with US-5485019A (post-published US equivalent)
D6: US-5198379A

IV. At oral proceedings before the board, the appellant requested that the decision under appeal be set aside and that a patent be granted on the basis of the main request or the auxiliary request filed with the statement of the grounds of appeal.

V. Claim 1 of the main request reads as follows

"*1. A semiconductor device comprising:*

a substrate (301);

an active matrix circuit formed on said substrate, said active matrix circuit comprising a first thin film transistor (337); and

a driving circuit formed on said substrate for driving said active matrix circuit, said driving circuit comprising a plurality of second thin film transistors (335, 336) each comprising an n-channel thin film transistor (335),

wherein said first thin film transistor (337) and said n-channel thin film transistor (335) has a channel region, source and drain regions, and at least one high resistance region having a higher resistance than the source or drain regions,

and the extent of the high resistance regions in the direction between the source and drain regions in said first thin film transistor (337) is larger than that in said n-channel thin film transistor (335),

characterised in that

said high resistance regions comprise lightly doped source/drain regions (317, 319) in which the concentration of dopant impurity is lower than the concentration of dopant impurity contained in said source and drain regions; and

the extent of the lightly doped source/drain regions in the direction between the source and drain regions in said first thin film transistor (337) is larger than that in said n-channel thin film transistor (335)."

VI. Claim 1 of the auxiliary request reads as follows:

"*1. A semiconductor integrated circuit comprising:*

a substrate;

at least one thin film transistor formed over the substrate which has first high resistance regions and first source and drain regions adjacent to the first high resistance regions; and

at least one other thin film transistor formed over the substrate which has second high resistance regions and second source and drain regions,

wherein a width of the first high resistance regions is larger than that of the second high resistance regions, and

wherein the first source and drain regions and the second source and drain regions comprise a metal silicide."

VII. In support of the application the appellant argued as follows:

The examining division objected to the feature that the plurality of second thin film transistors (TFTs) comprise a p-channel TFT as containing added subject-matter. This feature was now deleted from both the main and the auxiliary requests.

As regards the main request, those features which were added to claim 1 during examination in order to

distinguish the claimed invention from the prior art found a clear and unambiguous basis in the original application, in particular in the description of Figs. 5A to 5E.

The document considered by both the applicant and the examining division to constitute the closest prior art was document D4.

The features which distinguished the invention claimed in claim 1 from this nearest prior art were those set out in the characterising portion of claim 1. They were that the high resistance regions comprised lightly doped source/drain regions in which the concentration of dopant impurity was lower than the concentration of dopant impurity contained in the source and drain regions; and that the extent of the lightly doped source/drain regions in the direction between the source and drain regions in the first TFT was larger than that in the n-channel TFT.

The objective technical problem derived from these differences between the claimed invention and D4 was to improve the characteristics of a semiconductor device comprising an active matrix circuit TFT and driving circuit TFTs.

The claimed solution providing lightly doped source/drain regions improved the ON-OFF ratio of TFTs. In contrast the offset regions in document D4 were merely extensions of a channel region such that the resistivity is generally high, resulting in a desirable reduction of the OFF current but also an undesirable reduction in the ON current.

Moreover, the different extent of the lightly doped source/drain regions provided the further advantage that decreased the OFF current of the TFT of the active matrix and increased the ON current of the n-channel TFT of the driving circuit. In the case of a TFT of an active matrix circuit, it was particularly important to have a small OFF current in order to retain electrical charges in an associated pixel electrode during the refreshing period of a frame. On the other hand, the TFTs of a driving circuit required a large ON current capability. Hence, the lightly doped source/drain regions of the active matrix circuit TFT should be larger than those of the driving circuit TFTs.

The examining division reasoned that (starting from document D4) it would have been obvious to the skilled person in view of prior art document D6 to use lightly doped source/drain regions instead of offset regions. However, document D6 proposed the use of offset regions in order to reduce OFF currents. While document D6 admittedly referred to the alternative possibility of using an LDD (Lightly Doped Drain) structure in order to reduce OFF currents and improve the on/off ratio, this approach was dismissed in document D6 because an LDD structure would create a series resistance which (undesirably) reduced the ON current. The use of an LDD structure was thus described as disadvantageous compared with the proposed use of offset regions and hence document D6 taught away from using an LDD structure.

For these reasons, claim 1 of the main request involved an inventive step.

Claim 1 of the auxiliary request was based on originally filed claims 4 to 8 and 20 to 23, with the added feature that the first source and drain regions and the second source and drain regions comprised a metal silicide. The basis for this additional feature could be found in column 14, lines 1 to 5 of the application as published. The claim therefore complied with Art. 123(2) EPC.

Reasons for the decision

1. Admissibility of the appeal

The application was refused on the ground that no allowable set of claims was on file. In its decision, the examining division suggested that amended main claims directed to the embodiment of Figures 5A - 5E would be allowable (point 3.4 of the decision). The claims submitted with the statement of the grounds of appeal were according to the appellant based on this embodiment and therefore seek to overcome the objections raised in the decision under appeal (see "Case Law". 6th Ed, Chapter VII.D.7.5.2(d)).

The appeal is therefore admissible.

The main request

2. Novelty and inventive step

2.1 There is no dispute that document D4 presents the closest prior art (any reference to document D4 below

is to the US family document). Document D4 discloses a semiconductor device having the features of the pre-characterising part of claim 1 (see column 7, lines 45-61).

2.2 Document D4 discloses in quite general terms that separating the gate electrode from at least one of the source or drain regions prevents high electric field concentrations and hence breakdown of the gate insulating film (col. 7, lines 23 to 28).

2.3 Document D4 further discloses that the size of the offset determines the characteristics of a transistor. If the offset is large, the dielectric strength of the transistor is high, source drain leakage currents are small, but the mobility is low. In contrast, if the offset is small, mobility is high but dielectric strength is low. Choosing the size of the offset permits the formation of transistors with significantly different characteristics on the same substrate. Slow transistors with small leakage currents are suited for the active matrix in an LCD matrix display, fast transistors with small offsets are used in circuits peripheral to the display (col.7, lines 38 to 61). The slow and fast transistors referred to in document D4 fulfil the same function as the pixel control TFT (337) and the n-channel TFT (335) of the application of the application and correspond to the first thin film transistor and the n-channel thin film transistor of claim 1, respectively. Although not specifically referred to as such, the board finds no reason to doubt that the n-channel thin film transistor (335) of claim 1 falls into the category of "*TFT for peripheral circuits which must be driven fast*" of document D4

(col. 7, lines 55-57). The board accordingly concurs with the similar findings of the examination division (paragraph 3.2.2 of the decision under appeal) in this respect.

2.4 The device claimed in claim 1 of the application differs from the device disclosed in document D4 in two aspects. They are

(a) that the high resistance regions comprise lightly doped source/drain regions (317, 319) in which the concentration of dopant impurity is lower than the concentration of dopant impurity contained in the source and drain regions; and

(b) that the extent of the lightly doped source/drain regions in the direction between the source and drain regions in the first TFT (337) is larger than that in the n-channel TFT (335).

2.5 From these features it follows that the technical problem addressed by the application relates to decreasing the leakage current in the first transistor without degrading the performance of the n-channel transistor (published application, column 1, line 55 to column 2, line 21).

2.6 Document D6 (col. 2, lines 36-58 and col. 5, lines 24-32) compares prior art offset regions with prior art lightly doped regions. The offset regions are said to present difficulties in aligning the channel with the underlying gate electrode. The alternative of using lightly doped regions creates a series resistance which reduces the transistor ON current.

2.7 The appellant argued that document D6 taught away from replacing offset regions with lightly doped regions on account of the stated disadvantage of lower ON currents of lightly doped regions.

2.8 The board does not find this argument persuasive. Document D6 compares the perceived disadvantages both of prior art offset regions (difficulty of alignment) and prior art lightly doped regions (decreased ON current). Offset regions are said to reduce OFF currents, lightly doped regions to reduce OFF currents and improve the ON/OFF ratio. Document D6 then proposes its own solution for improving the technique for forming offset regions. In the board's view, the simple comparison of the disadvantages of two alternative prior art techniques cannot be considered to teach away from one or the other possibility, i.e., lightly doped regions or offset regions.

2.9 Hence the board agrees with the examining division, that replacing an offset region by a lightly doped region is known from document D6 and amounts to no more than choosing between two equivalent alternatives.

2.10 The skilled person faced with the task of reducing leakage currents in the first transistor while improving the ON current in the n-channel transistor would in the light of the above consider replacing offset regions with low doped regions.

2.11 On this point the board disagrees with the suggestion made by the examining division, that a claim to the embodiment of Figures 5A-5E would be patentably

different from the cited prior art. Given that replacing an offset region by a lightly doped region is itself known from document D6, it requires nothing further then to consider making the lightly doped regions of different size where in document D4 the offset regions were of different size if the aim is the same, i.e. to achieve different operating characteristics between the fast driving circuit transistors (335) which require a large ON current and hence a small lightly doped region, and the slow the pixel TFTs (337) which should have a low leakage current when in the OFF-state.

2.12 For the foregoing reasons, the board concludes that the subject matter of claim 1 of the main request does not involve an inventive step within the meaning of Art. 56 EPC 1973.

The Auxiliary request

3. Amendment (Article 123(2) EPC)

3.1 The appellant stated that the claims of the auxiliary request were based on original claims 4 to 8 and 20 to 23, with the addition in claim 1 that the first source and drain regions and the second source and drain regions comprise a metal silicide. This feature found its basis in the paragraph spanning original description pages 18 and 19.

3.2 The above-mentioned paragraph contains the sole mention of the formation of metal silicide which reads as follows: "*Furthermore, a film of a metal such as titanium, nickel, molybdenum, tungsten, platinum, or*

palladium is formed. For example, a titanium film 320 having a thickness of 50 to 500 ANGSTROM is formed by sputtering. As a result, the titanium film 320 is in contact with the regions 314 to 316 (Fig. 5D). A KrF excimer laser having a wavelength of 248 nm and a pulse width of 20 ns is irradiated to react the titanium film with the silicon in the active layer, thus forming metal silicide (titanium silicide) regions 330 to 332. ..." [emphasis added by the board]

Absent the feature that the first source and drain regions and the second source and drain regions comprise a metal silicide, claim 1 of the auxiliary request embraces all the described embodiments, not just the embodiment of Figure 5A to 5E. On the other hand, the description of the formation of the metal silicide film relates is not just confined to the embodiment of Figure 5 but specifically relates to the device regions 330 to 332 of Figure 5D being source/drain regions having adjacent lightly doped source/drain regions (see main request). The description does not contain any other references of any kind to forming metal silicide anywhere else. Furthermore, it would even appear that other embodiments would not be compatible with the feature of having the source and drain regions made of metal silicide. Hence the board finds that there is insufficient basis in the application as filed for the general statement in claim 1 that "*the first source and drain regions and the second source and drain regions comprise a metal silicide.*"

The board therefore concludes that claim 1 of the auxiliary request includes subject matter which extends

beyond the content of the application as filed and hence does not comply with the requirements of Article 123(2) EPC.

Order

For these reasons it is decided that:

1. For these reasons it is decided that:

2. The appeal is dismissed.

Registrar Chair

S. Sánchez Chiquero G. Eliasson