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Datasheet for the decision of 1 October 2008

Case Number: T 1506/05 - 3.5.01

Application Number: 96101118.6

Publication Number: 0726538

IPC: G06F 17/50, G06F 11/263

Language of the proceedings: EN

Title of invention:
Topology-based computer-aided design system for digital circuits and method thereof

Applicant:
FUJITSU LIMITED

Opponent:
-

Headword:
Logic design verification/FUJITSU

Relevant legal provisions:
EPC Art. 123(2)

Relevant legal provisions (EPC 1973):
-

Keyword:
"Added subject-matter (yes)"

Decisions cited:
-

Catchword:
-

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Case Number: T 1506/05 - 3.5.01

D E C I S I O N
of the Technical Board of Appeal 3.5.01
of 1 October 2008

Appellant: FUJITSU LIMITED
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Decision under appeal: **Decision of the Examining Division of the European Patent Office posted 13 July 2005 refusing European application No. 96101118.6 pursuant to Article 97(1) EPC 1973.**

Composition of the Board:

Chairman: S. Steinbrener
Members: R. R. K. Zimmermann
G. Weiss

Summary of Facts and Submissions

I. European patent application no. 96 101 118.6 (publication no. 0 726 538) relates to computer aided design systems and methods for logic design verification. The application was refused by the examining division. According to the reasons given in writing by a letter posted on 13 July 2005, the application did not meet the requirements of Articles 83, 84, and 123(2) EPC 1973.

II. The appellant (applicant) lodged an appeal against the refusal of the application on 12 September 2005. On 11 November 2005, by a letter dated 10 November 2005, the grounds of appeal and a set of amended claims were filed, claim 1 reading as follows:

"A method using a computer-aided design system for logic design verification using a group of logic gates with implications, by analysing a first and a second separate digital circuit topology each comprising a set of primary outputs interconnected with logic gates, the logic gates being interconnected by wires, the topologies having a set of implications associated with the logic gates, each such primary output for each separate topology having a corresponding primary output on the other of the separate topologies, comprising the steps of:

selecting (213, 217) a tentative cut selection region (IP) in one of the separate topologies and a reflection tentative cut selection region (IP') in the other of the separate topologies, each of the separate topologies having one or more primary outputs and one or more corresponding primary outputs respectively;

said selecting step (213, 217) comprising:

selecting the tentative cut selection region (IP) in one of the separate topologies by selecting an output gate, being a logic gate at a primary output, in the one of the separate topologies, and the logic gates in the fan—in of that output gate that have implications in the one of the separate topologies or the other of the separate topologies by selecting said output gate as a selected gate and recursively, for each input gate to the output gate, determining if an input gate to the selected gate has implications in the one of the separate topologies or the other of the separate topologies and selecting the input gate as the selected gate until logic gates with implications in the one of the separate topologies or the other of the separate topologies for each input gate to the output gate are found, and selecting the reflection tentative cut selection region (IP') in the other of the separate topologies by selecting a set of logic gates in the other of the separate topologies by mapping implications in the tentative cut selection region to corresponding implications in the other of the separate topologies;

modifying (214, 215, 218, 219) the selected region (IP') in the other separate topology to obtain a complete cut, such that every point on the cut has an implication on the cut or between the cut and the primary outputs in the one of the separate topologies or in the other of the separate topologies;

said modifying step comprising:

marking (240) logic gates in the other of the separate topologies that can be reached from the output gate and that cannot be reached from one of the associated implications stored in the reflection

tentative cut selection region (IP') and storing (242) a representation of the marked logic gates as a set of candidate points;

marking (243) logic gates in the set of implications for the other of the separate topologies wherein each such logic gate has an associated implication on the cut or between the cut and the primary outputs in the separate topology or in the other of the separate topologies and storing (245) a representation of the marked logic gates in a further set of candidate points; and

marking (249, 264, 251) logic gates stored in both the set of candidate points and the further set of candidate points and storing a representation of those logic gates in the reflection tentative cut selection region; and

verifying (227) whether each of the topologies is equivalent by XORing together the corresponding primary outputs from the selected regions in each of the separate topologies using means for XORing;

said verifying step (227) comprising:

determining the effect of injecting Boolean values into the wires for each of the logic gates along the cut in the tentative cut selection region (IP) and along the cut in the reflection tentative cut selection region (IP') to thereby determine an output signal indicating equivalency asserted by the XORing means."

III. In a communication annexed to summons to oral proceedings requested by the appellant as an auxiliary measure, the Board indicated as its provisional opinion that it considered the examining division to be essentially right in refusing the application. In addition, it inter alia raised objections under

Article 123(2) EPC against the amendments of claim 1, in particular in respect to the feature "modifying... to obtain a complete cut" in claim 1, 5th paragraph.

IV. In a letter dated 22 July 2008, the appointed representative informed the Board that the appellant had lost interest in the application and would not be represented at the oral proceedings.

V. The oral proceedings were held on 1 October 2008 as scheduled. The appellant did not appear at the oral proceedings.

The case was considered by the Board on the basis of the requests filed in writing that the decision under appeal be set aside and that a patent be granted on the basis of claims 1 to 30 submitted with the statement setting out the grounds of appeal by letter dated 10 November 2005. After deliberation, the Board closed the debate and announced the decision on the appeal.

Reasons for the Decision

1. The appeal is admissible.

2. The appeal is not allowable, however, for the reason that the amendments of claim 1 do not meet the requirements of Article 123(2) EPC. As a consequence of this deficiency, the further issues of clarity of claims and sufficiency of disclosure as raised in the decision under appeal are not any more material and are thus not further pursued in the present decision on the appeal.

3. The Board already raised doubts regarding the original disclosure of the method step "modifying (214, 215, 218, 219) the selected region (IP') in the other separate topology to obtain a complete cut" (see point III above).

4. There is clearly no literal basis for this wording in the application as originally filed. The reference numbers 214, 215, 218, and 219 refer to the preferred embodiment of the logic design verification shown as flowchart in figures 16A and 16B and to the corresponding text portions of the description, in particular to col. 18, line 12 ff., col. 19, line 33 ff., col. 26, line 54 ff., col. 28, line 44 ff., col. 31, line 16 ff. and line 47 ff.

From neither one of these text passages follows, directly and unambiguously, the modifying step in issue. The flowchart of figure 16A rather implies that the separate topologies (circuit 1 and circuit 2) are analysed separately to create a tentative cut selection region and a corresponding reflection region mapping to the other respective circuit separately for each topology and, consistently, to produce "a pair of cuts", as described at col. 20, line 34 to col. 21, line 20, for example. Despite the doubts raised by the Board in its communication, the appellant did not forward any arguments helpful in clarifying the situation (see point IV above). Considering these circumstances of the present case, the Board determines that the requirements of Article 123(2) EPC are not fulfilled.

Order

For these reasons it is decided that:

The appeal is dismissed.

The Registrar: The Chairman:

T. Buschek S. Steinbrener