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Case Number: T 1472/05 - 3.5.02

Application Number: 97101923.7

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Title of invention:
Depuncturing circuit

Applicant:
Kabushiki Kaisha Kenwood

Headword:
-

Relevant legal provisions:
EPC Art. 56

Relevant legal provisions (EPC 1973):
-

Keyword:
"Inventive step - no (all requests)"

Decisions cited:
-

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Case Number: T 1472/05 - 3.5.02

D E C I S I O N
of the Technical Board of Appeal 3.5.02
of 29 January 2008

Appellant: Kabushiki Kaisha Kenwood
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Decision under appeal: **Decision of the Examining Division of the European Patent Office posted 7 July 2005 refusing European application No. 97101923.7 pursuant to Article 97(1) EPC.**

Composition of the Board:

Chairman: M. Ruggiu
Members: M. Rognoni
P. Mühlens

Summary of Facts and Submissions

I. The appellant (applicant) appealed against the decision of the examining division refusing European Patent application No. 97 101 923.7.

II. In the contested decision, the examining division found, *inter alia*, that the subject-matter according to the claims of the main and first auxiliary requests did not involve an inventive step within the meaning of Article 56 EPC, because it followed in a straightforward and obvious manner from the following document:

D1: ETS 300 401, "Radio broadcasting systems; Digital Audio Broadcasting (DAB) to mobile, portable and fixed receivers", February 1995, pages 141 to 149.

As to the auxiliary requests 2 and 3, they were filed as a matter of precaution in case the examining division did not accept the correction of "*block number count g'* " into "*bit number count g'* ". As the examining division accepted this correction, the auxiliary requests 2 and 3 were not considered in the contested decision.

III. In a communication dated 21 September 2007 accompanying the summons to attend oral proceedings, the Board observed, *inter alia*, that the claim of the main request did not seem to be clear within the meaning of Article 84 EPC and that the claims of the auxiliary requests 1 to 3 appeared to include expressions which were either unclear or not supported by the application

documents as originally filed (Articles 84 and 123 (2) EPC). As to the question of inventive step within the meaning of Article 56 EPC, the Board referred to the following documents:

D2: US-A-5 029 331
D3: US-A-5 438 590

IV. With a letter dated 28 December 2007, the appellant filed a new method claim by way of auxiliary request 4.

V. Oral proceedings before the Board were held on 29 January 2008.

VI. The appellant requested that the decision under appeal be set aside and that a patent be granted on the basis of the main request or on the basis of one of the auxiliary requests 1 to 3, all filed with letter dated 25 April 2005, or on the basis of auxiliary request 4 filed with letter dated 28 December 2007.

VII. The single claim of the main request reads as follows:

"A depuncturing circuit comprising:

write address generator means (12) for generating a write address;

first memory means (11) for storing a convolutional code changing its code rate in unit of block at a write address generated by said write address generator means (12);

a counter (13) for counting the number of blocks;

second memory means (14) for storing in advance index information representative of a level of an error correction procedure and a corresponding block number and puncturing pattern information to be used a plurality of times corresponding to the block number;

read control means (16) for designating a read address through a selective count operation based on the puncturing pattern information and reading data from said first memory means at the designated read address;

selector means (17) for selecting either the data read from said first memory means in accordance with the contents of the puncturing pattern information or dummy data if the data read from said first memory means is not selected;

puncturing pattern read means (15) for reading the puncturing pattern information from said second memory means (14) by referring to the index information until the block number counted by said counter (13) reaches the block number stored in said second memory means (14) and sending the read puncturing pattern information to said read control means and said selector means (17); and

serial/parallel converter means (18) for converting a serial output of said selector means (17) and the puncturing pattern information into a parallel output and supplying the parallel output to a convolutional code decoder, wherein

said counter (13) is adapted to receive a read clock signal (f) and is adapted to output a bit number count (g') to said puncturing pattern read means (15)."

The single claim of the auxiliary request 1 reads as follows:

"A depuncturing circuit which receives a punctured convolutional code signal and its related control signal to reproduce an original convolution code signal, the punctured convolution signal being obtained by puncturing the original convolution code signal completed in unit of a frame consisting of a plurality of data blocks using several punctured patterns changing in unit of block, the depuncturing circuit comprises:

read/write memory means (11) for storing the received punctured convolution code signal (6) in unit of frame, the read/write memory means operating to read out a prior frame of the punctured convolution code signal while writing a present frame of the punctured convolution code signal;

write address generating means (12) for providing a write address (e) to the read/write memory means (11);

counter means (13) for counting the number of data bits in the received punctured convolution code signal to output a block number (g) indicative of an order of the block in one frame;

a first look-up table (14) for storing a correspondence table indicative of the correspondences between indexes

representative of error correctional procedures and puncturing indexes (P1) representative of the punctured patterns, each of the punctured patterns being determined for a specific group of blocks in one frame, the first look-up table (14) being responsive to both index information (h) included in the received control signal and the block number (g) outputted from the counter means (13) to identify and output a puncturing index (i) determined for a specific group to which a present data block belongs;

a second look-up table (15) for storing a correspondence table indicative of the correspondences between the puncturing indexes (PI) and the puncturing patterns, the second look-up table being responsive to the puncturing index (i) outputted from the first look-up table (14) to operate so as to sequentially output a puncturing enable signal (j) corresponding to the puncturing pattern represented by the puncturing index (i);

read control means (16) for providing a read address (k) to the read/write memory means (11), the read control means being responsive to a logic level of the puncturing enable signal (j) from the second look-up table (15) to operate so as to selectively increment the read address of the read/write memory means (11);

selection means (17) adapted to receive outputs from both the read/write memory means (11) and the second look-up table (15), the selection means (17) being responsive to the puncturing enable signal (j) to select either a received data bit (e) outputted from the read/write memory means (11) or a dummy data bit (m)

as to sequentially output the selected bit as a serial signal (n); and

serial/parallel converter means (18) for converting the serial signal (n) outputted from the selection means (17) and the puncturing enable signal (j) outputted from the second look-up table (15) to respective parallel signals and to transmit the respective parallel signals to a convolutional code decoder, wherein

said counter means (13) is adapted to receive a read clock signal (f) and is adapted to output a bit number count (g') to said second look up table (15)."

The auxiliary requests 2 and 3 differ from the main request and the auxiliary request 1, respectively, in that the expression "bit number count (g')" of the latter is replaced by "block number count value (g')".

The single claim of the auxiliary request 4 reads as follows:

"Method for depuncturing, comprising the following steps:

a burst input of data (b), corresponding to a frame of encoded and punctured data bits, is written in a first memory (11), having a capacity of two frames, at addresses defined by a write address generator (12), which is essentially a counter incremented in response to an input data clock signal (d),

the time basis for depuncturing the received data frame is provided by a read clock signal (f) which directly or indirectly controls a read address generator (16) for retrieving data stored in said first memory (11), a PI creating circuit (14) and a puncturing enable creating circuit (15) for determining if a particular bit of the depunctured data stream is a bit of the received frame or a dummy bit, and a serial/parallel convertor (*sic*) means (18),

information relating to the depuncturing procedure to be used for a particular frame is provided by an index information signal (h),

said read clock signal (f) is fed to a block number counter (13) which outputs a seven bit block number count (g') indicative of the bit number within one block and a nine bit block number (g) indicative of the block number within a frame,

said nine bit block number (g) and said index information signal (h) are used in said PI creating circuit (14) to identify a puncturing index (i) on the basis of respective data stored in advance,

said seven bit block number count (g') is used together with said puncturing index (i) to identify in the puncturing enable creating circuit (15) the elements of a corresponding puncturing vector stored in said puncturing enable circuit (15) and used to generate a corresponding puncturing enable signal (j),

said read address generator (16), which counts said read clock signal (f) when the puncturing enable

signal (j) is high, outputs a read address (k) to identify the data bit (l) stored in said first memory (11) and thus not suppressed by puncturing,

said data bit (l) read from said memory circuit (11) at the read address (k) is fed to a selection circuit (17),

said selection circuit (17) selects the data bit (l) when the puncturing enable signal (j) is high and selects dummy data (m) when said puncturing enable signal (j) is low, and

said puncturing enable signal (j), which can be used as an erase signal for a Viterbi decoder, is supplied together with the selected data (n) to said serial/parallel convertor (*sic*)18."

VIII. The appellant's arguments relevant to the present decision may be summarised as follows:

The present application dealt with the problem of realizing a depuncturing circuit applicable to a digital audio broadcasting system (DAB) conforming to the European specifications set out in D1. The proposed solution consisted essentially in using separate circuits 14 and 15 for storing the lookup tables which defined the puncturing rules of the DAB specifications (see Figures 11 to 14 of the application as published), and in addressing the stored lookup tables by means of a block number count g and a bit number count g' generated by a single counter 13.

The skilled person, however, understood that a depuncturing circuit compatible with the puncturing procedure according to D1 could be solved in many different ways. For instance, it would be possible to use a single counter which generated a bit number count g' for addressing a lookup table based on a combination of the lookup tables of Figures 11 to 14. This solution had the advantage that no further count, such as the block number count g, and therefore no synchronisation was necessary.

According to a further solution, the two lookup tables of Figures 11 to 14 could be addressed by two separate counters which received the same read clock signal. It would also be possible to provide a single counter 13, which delivered the bit number count g' to the lookup table stored in the circuit 14, and to have circuit 15 responsive only to the output of the circuit 14. Furthermore, the block number counter 13, the PI creating circuit 14 and the puncturing enable creating circuit 15 could be replaced by a software based solution.

Another option available to the skilled person would be to design a circuit for clocking the depuncturing process on the basis of the index signal IDX, which contained all information required to select the appropriate depuncturing vector. However, if adopted for codes of the DAB specifications, this approach would give rise to synchronization problems, since DAB codes were arranged in blocks with variable code rates.

Already the fact that many different solutions to the problem of realising a circuit complementary to the

puncturing specified in D1 were possible showed that the depuncturing circuit or method according to the present invention did not follow in a straightforward manner from D1. In fact, the inventor had found that the best solution was the one set out in the present claims because it overcame all synchronization problems and was very flexible as far as possible modifications of the puncturing patterns were concerned.

As to the cited prior art documents, the aim of D2 was to improve a system comprising a transmitter and receiver in order to attain higher processing speeds by parallel processing during puncturing and depuncturing. Furthermore, D2 was directed to a depuncturing process for data punctured using a comparatively simple puncturing rule with a constant code rate.

As the DAB specifications implied complex puncturing rules with code rates which changed in a unit of data block, the present invention had to rely on a complex circuit configuration. Thus, higher order bits (g) of a counter were used to define the puncturing index PI, and the defined PI and lower order bits (g') of the counter output were used to create a puncturing enabled signal (j) which was in turn used as a clock enable signal for the read address generator 16 (Figure 1 of the application). This approach for addressing the appropriate puncturing vectors and timing the depuncturing procedure was neither known from nor suggested by D2.

D3 disclosed a depuncturing circuit operated in such a way that a puncturing pattern was read out of a memory using a counter. The read puncturing pattern was then

used to perform a FIFO read processing which involved the insertion of dummy bits. The FIFO processing according to the present invention was substantially different in that it involved a buffer (memory circuit 11) holding two frames, a write address generator and a read address generator which were skilfully operated to input a received signal and to hold and process the received signal. The logic circuit according to the present application consisted of gate circuits, a counter and a memory circuit whose combination realised any needed function. In particular, the claimed invention was unique in the way the clock signals and control signals to be sent to the counter and memory circuit were created and provided.

Furthermore, also D3 was directed to a depuncturing process for data punctured according to a simple puncturing scheme which was not comparable with the ones of the DAB specifications.

In summary, D1 was directed to specifying a puncturing rule in the DAB system, while D2 and D3 disclosed simple depuncturing techniques which were irrelevant to the puncturing rule of D1. In particular, D2 and D3 were not aimed at executing a depuncturing process on a received punctured signal whose code rate changed in a unit of data block. In the light of this, it would have been impossible to apply the teachings of D2 and D3 to a system according to D1. However, even if had been applied, the result would not have corresponded to the present invention. Consequently, the subject-matter of the claims according to all requests involved an inventive step within the meaning of Article 56 EPC.

Reasons for the Decision

1. The appeal is admissible.

2.1 The present application is directed to a depuncturing circuit applicable to a digital audio broadcasting system (DAB) "*conforming with European Specifications*" (application as published, column 1, lines 7 to 13).

2.2 The European specifications DAB which are relevant to the present case can be summarised as follows:

- L bits of the original signal constituting one frame are converted into convolutional codes at a constraint length of 7 and a code rate of 1/4;

- the corresponding convolutionally coded frame comprises 4L bits and 6 x 4 bits obtained by encoding the 6 bits remaining in the six delay stages of the convolutional encoder after the last bit of the frame has entered the encoder (application as published: column 4, lines 7 to 34);

- the convolutionally encoded frame of L bits is then converted into 4 x (L+ 6) serial bits which are divided into blocks, each block having 128 bits and being divided into sub-blocks of 32-bits (column 4, lines 35 to 38);

- the four sub-blocks of a 128 - bit block are punctured by means of one of the predetermined puncturing vectors vPI, thus obtaining punctured

blocks with different code rates and correction abilities;

– all the blocks of an encoded frame are punctured according to the scheme illustrated in Figures 13 and 14 of the present application, where the index IDX is indicative of the audio bit rate, the protection level P, the numbers of successive blocks L1 to L4 to be punctured with corresponding puncturing vectors specified by the vector indexes PI_1 to PI_4;

– the puncturing vectors νPI are defined as shown in Figures 11 and 12;

– the last remaining 24 bits of a frame are punctured using a puncturing vector VT (PI = 31) which reduces their number to 12 bits ("tail bits");

In other words, the DAB specifications imply the conversion of a frame of L bits into a sequence of bit blocks at variable code rates (from 8/9 to 8/32 and 8/12 according to Figures 11 and 12) and the transmission of each frame as a burst signal together with its corresponding index IDX which identifies the puncturing scheme adopted to vary the code rate of the blocks in a frame.

2.3 As pointed out in the present application (published application: column 1, line 45 to column 2, line 19) depuncturing convolutional codes punctured in conformity with the DAB format presents some difficulty

because the received signal burst is made up of data blocks which have different code rates.

3.1 According to the description (application as published, column 1, lines 17 to 44), the starting point of the present invention was a depuncturing circuit as shown in Figure 15 of the application. In this circuit, a clock signal r for timing the Viterbi decoder, the null interpolation state decoder and thus the data readout from the buffer circuit 61 was reproduced from the clock signal x which synchronized the input codes.

Though the depuncturing circuit of Figure 15 was effective for data punctured at a fixed code rate, in the case of convolutional codes with variable code rates according to the DAB specifications, it would be difficult to derive a clock signal from a signal x which is synchronous with the input codes, whose rates in principle, could vary from block to block within the same frame.

The clock reproduction circuit 62 could be replaced by a master clock generator which produced a clock signal representing the least common multiple of the rates of the clock signal x (input of the buffer circuit 61) and of the clock signal r fed to the Viterbi decoder 63 and to the null interpolation circuit 65. However, as the DAB specifications involved 25 sets of code rates, the least common multiple was a very high frequency.

3.2 The gist of the present invention consists essentially in providing a clock signal ("read clock signal f", Figure 1) which is independent of the input data clock d and of the index IDX and thus of the variable code

rates of the data blocks in a received frame. The read clock f controls all the circuits involved in the generation of a depunctured bit sequence at the code rate of the originally convolutionally encoded data sequence (*i.e.* 1/4), and, in particular, generates the signals g' and i required for identifying the appropriate puncturing vectors.

4.1 The main request and the auxiliary requests 1 to 3 of the appellant relate to a depuncturing circuit as shown in Figure 1 of the present application, whereas the auxiliary request 4 is directed to a method which essentially reflects the operation of that circuit.

In spite of the objections raised in the Board's communication under Articles 84 and 123 (2) EPC and concerning the main request and the auxiliary requests 1 to 3, the essential question to be considered in the present appeal is whether the depuncturing circuit shown in Figure 1 of the application or a method based on its operation involves an inventive step within the meaning of Article 56 EPC.

4.2 With reference to Figure 1 and to the corresponding parts of the description, the essential features of the claimed circuits and method can be summarized as follows:

– the time basis for depuncturing the received data frame is provided by a *"read clock signal f"* which directly or indirectly controls the read address generator 16 (for retrieving data stored in the memory circuit 11), the "*PI creating circuit 14*" and the "*puncturing enable creating circuit 15*"

(for determining if a particular bit of the depunctured data stream is a bit of the received frame or a "*dummy bit*") and the serial-to-parallel converter 18;

– information relating to the depuncturing procedure to be used for a particular frame is provided by an "*index IDX*" as defined by the DAB specifications (see Figures 13 and 14);

– the read clock f is fed to the block number counter 13 which outputs a seven bit "*block number count value g'* " (or *"bit number count g' "*) indicative of the bit number within one block and a nine bit "*block number g"* indicative of the block number within a frame;

– the *"block number g"* and the index IDX are used in the PI creating circuit 14 to identify the puncturing index PI on the basis of the tables shown in Figures 13 and 14;

– the *"block number count value g'* " is used together with the "*puncturing index i"* to identify in the puncturing enable creating circuit 15 the elements of a corresponding puncturing vector stored in circuit 15 and used to generate a corresponding "*puncturing enable signal j"*;

– the read address generator 16, which counts the read clock f when the puncturing enable signal j is high, outputs a "*read address k"* to identify the data bit stored in the memory 11 and thus not suppressed by puncturing;

– the *"data bit l"* read from the memory circuit 11 at the read address k is fed to a "*selection circuit 17*";

– the selection circuit 17 selects the "*data bit l*" when the "*puncturing enable signal j*" is high and *"dummy data m"* when the signal *j* is low;

5.1 In support of the inventive step of the subject-matter of all requests, the appellant has essentially submitted that the depuncturing circuit and method of the present invention were not a straightforward solution to the problem of depuncturing applied to convolutional codes according to the DAB specifications. The index signal IDX associated with each data frame contained all the information required for determining the puncturing vector to be used for depuncturing a particular block of that frame. As the switching from one puncturing vector to the next was determined by the IDX signal, it would have been obvious to a skilled person to use this signal as a basis for timing the selection of the appropriate puncturing vector and the operation of the depuncturing circuit.

5.2 In the appellant's opinion, however, the present invention took a different approach and thus avoided all the problems relating to the variable code rates of the bit blocks by relying on a read clock signal which was not generated on the basis of the index IDX or of the code rates of the blocks.

6.1 According to the DAB specifications, a block of 128 encoded bits having a code rate of 1/4 is punctured by

means of a puncturing vector of 32 bits applied to each of the frame's four sub-blocks of 32 bits. As shown in Figures 11 and 12, depending on the puncturing vector, the code rate can vary from 8/32 (*i.e.* 1/4 when in effect no puncturing is performed) to 8/9 (when only 9 bits out of 32 are retained).

The purpose of a depuncturing procedure is to combine the received data stream with "dummy-bits", which replace the punctured bits, in order to generate a bit stream having the original code rate (*i.e.* 1/4 in the present case).

As the depunctured data stream has a constant and predetermined code rate, it is obvious to assume that the clock signal necessary for addressing the depuncturing pattern, driving the circuit which selects the received bits or the "dummy-bits" or controlling the Viterbi decoder should also be constant and determined on the basis of the code rate of the depunctured data stream to be decoded (see D2, Figure 15 and D3, Figure 3).

6.2 Thus, in the opinion of the Board, the person skilled in the art wishing to develop a depuncturing circuit for convolutional codes encoded and punctured according to the DAB specifications would not start from a circuit according to Figure 1 of the present application but from a circuit which used a locally generated clock signal at a predetermined frequency independent of the code rate of the received data blocks, as known from D2 and D3.

7.1 Figure 15 of D2 shows the principle of a parallel depuncturer using a depuncturing pattern stored in a memory Sp2. A clock CLK 1 provides the time basis for generating a bit stream having the same code rate as the encoded signal prior to puncturing. The clock signal CLK1 thus cyclically addresses the stored depuncturing pattern by means of a multiplexer MX5 controlled by a clock counter. The output of an AND gate G5, which combines the depuncturing pattern and the clock signal CLK1, controls the readout of the memory FIFO-D and a multiplexer MUX-D disposed downstream of the FIFO-D in order to insert "dummy bits" into the bit stream read out of the FIFO-D in correspondence with the 0's of the depuncturing pattern.

As shown in Figure 15, the clock signal CLK1 is not related to the received signal and, in effect, the write and read operations of the memory FIFO-D used for storing the received data are controlled by independent clocks.

7.2 Figure 3 of D3 shows also a depuncturer which operates according to the same principle and comprises a "*symbol clock*" for writing the received data stream into a FIFO 312. An independent "*data clock*" addresses via a counter 322 a depuncturing pattern stored in a ROM 326 and times the bit sequence read out of the FIFO 312, whereby, as explained in D3 (column 17, lines 26 to 29 and column 17, line 55 to column 18, line 11), the FIFO 312 outputs a bit of the stored bit sequence or a "dummy-bit" X in dependence of a 1 or a 0 of the stored puncturing pattern.

7.3 It is obvious to a person skilled in the art that a circuit for depuncturing data encoded according to the DAB specifications must account for the fact that there are 64 possible ways of puncturing a frame of encoded data, as defined by the index IDX, and that there are 25 possible ways of puncturing a block in a frame, as indicated by the puncturing index PI.
Furthermore, as the selection of the depuncturing vector to be used for a particular block of a frame of index IDX depends on the position of the block in the frame, it is obvious that both the index IDX and a block count are necessary to address the appropriate depuncturing vector.

7.4 In other words, a circuit for depuncturing data encoded and punctured according to the DAB specification must comprise the following features:

- means (see PI creating circuit 14 of Figure 1) for storing all puncturing schemes defined by the indexes IDX,

- means for addressing the appropriate puncturing vector as a function of the index IDX and of a block number count,

- means for storing all puncturing vectors and sequentially addressing the 32 bits of the selected vector, whereby a 32 - bit vector is applied to each of the 4 sub-blocks and thus addressed 4 times.

7.5 D3 (see Figure 3, column 17, lines 49 to 54) teaches, *inter* alia, to control the depuncturing pattern by

means of a signal derived for instance from the transmitter at the time a transmission sequence begins. In the case of the DAB specifications such signal would be provided by the index IDX. However, since the DAB specification defines a puncturing vector also as a function of the position of a block in a frame, it would be obvious to a person skilled in the art, wishing to apply the depuncturing principle shown in D3 to the DBA specifications to provide means for counting the blocks in a frame. A block number count can be readily performed by the counter already used to count 4 times the bits of the 32-bit depuncturing pattern applied to each sub-block of a data block, once it is considered that a block of punctured code always corresponds to a 128-bit block of depunctured code.

7.6 In summary, the Board considers that the means or method steps for selecting the depuncturing pattern as a function of the index IDX and of the block number count according to the present invention is a straightforward application of the depuncturing principle known from D2 or D3 to a punctured convolutional code according to the DAB specification.

8.1 It could be argued that the subject-matter of the appellant's requests comprises further features which distinguish it from the circuits known from the available prior art. In fact, Figure 15 of D2 shows an "*elastic memory*" FIFO-D instead of an addressable memory 11 for storing two frames to be depunctured (see Figure 1 of the application), whereas the FIFO 312 according to Figure 3 of D3 includes the functionality of the selection circuit 17 of the invention which

inserts "dummy-bits" in correspondence to the 0's of the puncturing pattern.

Furthermore, the claimed circuit has a serial/parallel converter for converting a serial output of the selection circuit 17 and the puncturing pattern into a parallel output and for supplying the parallel output to a convolutional code decoder.

8.2 There could be no doubt, however, that also the addressable memory circuit 11 of the present invention is essentially used as a buffer and that the bits of a stored frame are read out in the same order as they are read in. Thus, its functionality is not different from the one of an elastic FIFO. As to the possibility of storing two frames, it is a well-known measure adopted when data are transmitted in bursts, as in the case of the DAB specifications.

As to the serial/parallel converter of the invention, Figure 3 of D3 comprises a demultiplexer 342 which converts a serial data stream read out of the FIFO 312 into two parallel streams G1 and G2. Furthermore, D3 (column 18, lines 33 to 36) points out that the *"presence of the dummy bits is signalled to Viterbi decoder 66 by the output of multiplexer 332 by a 0 at the output of the multiplexer", i.e.* by the puncturing pattern.

8.3 In summary, the Board finds that it would have been obvious to a person skilled in the art, wishing to develop a depuncturing circuit or method for the DAB specifications according to D1, to adapt the teaching of D2 or D3 to the puncturing schemes set out in D1. In

doing so, the skilled person would have arrived at a circuit or a method falling within the terms of the claims of the appellant's requests. Thus, the subject-matter of these claims does not involve an inventive step within the meaning of Article 56 EPC.

9. In the result, none of the appellant's requests is allowable and the Board sees no possibility of amending the claims on file so as to meet the requirement of Article 56 EPC. Hence, the application has to be refused.

Order

For the above reasons it is decided that:

The appeal is dismissed.

The Registrar: The Chairman:

U. Bultmann M. Ruggiu