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Datasheet for the decision of 27 March 2008

Case Number: T 1357/05 - 3.4.03

Application Number: 02744333.2

Publication Number: 1402568

IPC: H01L 21/288

Language of the proceedings: EN

Title of invention:
Method and apparatus for controlling a plating process

Applicant:
ADVANCED MICRO DEVICES, INC.

Opponent:
-

Headword:
-

Relevant legal provisions:
EPC Art. 56

Relevant legal provisions (EPC 1973):
-

Keyword:
"Inventive step (no)"

Decisions cited:
-

Catchword:
-

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Case Number: T 1357/05 - 3.4.03

D E C I S I O N
of the Technical Board of Appeal 3.4.03
of 27 March 2008

Appellant: ADVANCED MICRO DEVICES, INC.
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Decision under appeal: **Decision of the Examining Division of the European Patent Office posted 30 May 2005 refusing European application No. 02744333.2 pursuant to Article 97(1) EPC.**

Composition of the Board:

Chairman: R. G. O'Connell
Members: G. Eliasson
T. Bokor

Summary of Facts and Submissions

I. This is an appeal against the refusal of application 02 744 333 for lack of inventive step over the prior art evidenced by document

D2: "Introduction of Copper Electroplating Into a Manufacturing Fabricator," D. Chung et al., 1999 IEEE/SEMI Advanced Semiconductor Manufacturing Conference, pages 282 to 289

and common general knowledge in the art.

II. The appellant applicant requests that the decision under appeal be set aside and a patent granted on the basis of amended claims 1 to 10 sent with the statement of grounds of appeal.

III. Independent claim 1 with the amendments marked reads as follows:

"1. A method ~~of~~ **for** controlling a plating process in a semiconductor device comprising:

plating a process layer (160) on a wafer in accordance with a recipe ~~which includes the grain size of said process layer~~;

measuring a thickness of the process layer (160); and

determining at least one plating parameter of the recipe for subsequently formed process layers (160) based on the measured thickness; **and at least one**

dynamic range of the at least one plating parameter, the dynamic range being bounded by at least one grain size limitation."

IV. The appellant applicant's arguments can be summarized as follows:

(a) In its decision, the examining division admitted that document D2 did not disclose the step of determining at least one plating parameter of the recipe for subsequently formed process layers based on the measured thickness. To remedy this admitted deficiency in document D2, the examining division alleged that a skilled person would simply apply Faraday's law to relate time and current to thickness of a layer.

(b) It was also admitted in the decision that the process recipe described in document D2 did not account for grain size in the process layer. It was however alleged that any process engineer would be aware that changing the process parameters might change the grain size of the plated process layer. Accordingly, the examining division took the position that the skilled person would change the parameters of the plating process within these known limitations to obtain a deposited layer with the desired characteristics.

(c) A person of ordinary skill in the art would tend not to change the plating parameters automatically to avoid introducing grain size issues. Moreover, the cited prior art was silent with regard to any limitations that might be imposed on the plating

parameters by the grain size of the deposited material and was silent with regard to any dynamic ranges of the plating process parameters that might be imposed by practical grain size limitations. On the contrary, Faraday's law imposed no constraints on the range of the plating process parameters.

Reasons for the Decision

1. The appeal is admissible.

2. Claim 1 has been amended to include the step of determining at least one dynamic range of the at least one plating parameter, where the dynamic range is bounded by at least one grain size limitation, whereas in the version which formed the basis for the decision under appeal, it was merely stated that the recipe included the grain size of the process layer (see item III above). The amendment to claim 1 thus more clearly specifies that any changes made to the at least one plating parameter are subject to the constraint of meeting a previously specified grain size limitation (see the application, page 3, lines 25 to 28). The arguments presented by the appellant applicant in the statement of the grounds of appeal relating to this amendment, ie the effects a change in plating parameters might have on the grain size of the plating layer and whether the skilled person for this reason would refrain from changing the plating recipe (see item IV(c) above), have already been dealt with in the decision under appeal (see "Applicant's Arguments" in the decision under appeal). Hence the amendments to

claim 1 do not raise any new issues which were not dealt with in the decision under appeal, and therefore, the board is in a position to deliver a decision directly on the basis of the new claims (Article 12(3) of the Rules of Procedure of the Boards of Appeal).

3. *Inventive step*

3.1 Document D2 discloses a method of copper electroplating in a semiconductor device which includes a step of plating a process layer made of copper on a semiconductor wafer (see "Abstract" and "Introduction"). It is implicit for the person skilled in the art that the step of plating a process layer is in accordance with a "recipe" with carefully specified process parameters ensuring that the deposited copper films reliably meet the strict requirements set in a semiconductor manufacturing process.

It is mentioned in document D2 that the plating process obeys Faraday's law of electrolysis which means that the thickness of the deposited film is proportional to the product of the current density and the deposition time (see page 284, paragraph bridging left and right hand columns). The thickness of the deposited process layer is determined by measuring the sheet resistance of the process layer (page 284, last paragraph; Figure 6; page 286, left hand column).

3.2 The method of claim 1 differs from that of document D2 in that (A) at least one plating parameter of the recipe is determined for subsequently formed process layers based on the measured thickness; and (B) the

dynamic range of the plating parameter is bound by at least one grain size limitation.

Document D2 does not disclose any specific plating parameter to be adjusted in order to obtain the desired thickness.

3.3 Relative to D2, the technical problem solved by the claimed process is that of controlling a plating process so that the properties of the deposited film reliably remain within specification.

3.4 Regarding feature (A), document D2 mentions that the film thickness has to be kept within a range set by the requirements of guaranteeing adequate hole-filling of damascene structures and being compatible with the subsequent chemical-mechanical polishing process (page 286, left hand column). The thickness of the plated films is monitored using multiple-site sheet resistance measurements on a lot-by-lot basis (Figure 6).

The skilled person following the teaching of document D2 would understand that if the film thickness should fall outside of the acceptable range, the plating process would have to be adjusted accordingly. It is notorious in the field of electroplating that parameters such as deposition time, electrical current, and temperature of the plating bath directly affect the thickness of the plated layer. The skilled person would therefore as a matter of routine choose to vary at least one of the above parameters in order to obtain a plated layer having a thickness lying within the specified range.

3.5 As to feature (B), the skilled person would be aware that the dynamic range of the plating parameter to be adjusted is constrained by the requirement that other properties of the plated layer, notably the grain size, have to be kept within their respective specified ranges. This limitation in process parameter space imposed by design specifications is usually known in the art as the "process window". As the grain size of a metal interconnection structure is known to have a profound effect on phenomena such as electro-migration of a wiring layer, the skilled person would as a matter of course ensure that any changes in the plating parameters would not result in unacceptable changes in the grain size of the plated film.

3.6 The appellant applicant argued that the skilled person would tend not to change the plating parameters automatically in order to avoid introducing grain size issues and that the cited prior art was silent with regard to any limitations that might be imposed on the plating parameters by the grain size of the deposited material (IV(b) and (c) above).

3.6.1 The above arguments fail to persuade the board, since firstly, the skilled person would in any case have to change the plating parameters whenever the thickness of the plated film fell outside of the specified range. Secondly, it is common general knowledge in the art that the issue of grain size is of crucial importance for the quality of a wiring layer in an integrated circuit. Hence the skilled person faced with the task of developing an electroplating process to be used in fabrication of semiconductor integrated circuits would always have to pay attention to the grain size,

regardless of whether or not this issue was emphasised in document D2.

3.6.2 Furthermore, the description is also silent about the applicable grain size values, the methodology for measuring them, and in particular, how grain size changes with plating parameters. This implies that these factors were known to the skilled person.

3.7 For the above reasons, in the board's judgement, the subject matter of claim 1 does not involve an inventive step within the meaning of Article 56 EPC.

Order

For these reasons it is decided that:

The appeal is dismissed.

Registrar Chair

S. Sánchez Chiquero R. G. O'Connell