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**Datasheet for the decision  
of 16 November 2006**

**Case Number:** T 1031/05 - 3.4.01

**Application Number:** 97304646.9

**Publication Number:** 0816857

**IPC:** G01R 1/20

**Language of the proceedings:** EN

**Title of invention:**

Differential attenuator common mode rejection correction  
circuit

**Patentee:**

Tektronix Inc.

**Opponent:**

-

**Headword:**

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**Relevant legal provisions:**

EPC Art. 56

**Keyword:**

"Inventive step (yes) - after amendment"

**Decisions cited:**

-

**Catchword:**

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Case Number: T 1031/05 - 3.4.01

**D E C I S I O N**  
of the Technical Board of Appeal 3.4.01  
of 16 November 2006

**Appellant:** Tektronix Inc.  
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**Representative:** Burke, Steven David  
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**Decision under appeal:** Decision of the Examining Division of the  
European Patent Office posted 10 March 2005  
refusing European application No. 97304646.9  
pursuant to Article 97(1) EPC.

**Composition of the Board:**

**Chairman:** B. Schachenmann  
**Members:** R. Bekkering  
H. Wolfrum

## Summary of Facts and Submissions

- I. European patent application 97 304 646.9 (publication no. EP-A-0 816 857) was refused pursuant to Article 97(1) EPC by a decision of the examining division dispatched on 10 March 2005 on the grounds of lack of inventive step.
- II. Reference was *inter alia* made to the following documents:
- D1: US-A-4 663 586
- D2: H. Bonekamp, "Differential Probe for Oscilloscopes", Elektor Electronics, vol 20, no 222, May 1994, pages 22-25.
- D3: US-A-4 507 618
- III. The applicant (appellant) lodged an appeal against the decision on 20 May 2005 and paid the appeal fee on the same day. The statement setting out the grounds of appeal was received on 14 July 2005.
- IV. Oral proceedings, requested as an auxiliary measure by the appellant, were held on 16 November 2006.
- V. The appellant requested that the decision under appeal be set aside and a patent be granted on the basis of the following documents:

Claims: No. 1 filed at the oral proceedings on  
16 November 2006;  
Description: Pages 1 to 8 filed at the oral  
proceedings on 16 November 2006;  
Drawings: Sheets 1/2 and 2/2 filed at the oral  
proceedings on 16 November 2006.

VI. Claim 1 reads as follows:

*"1. A differential attenuator comprising:  
a positive input node (Vin-p);  
a negative input node (Vin-n);  
a positive output node (Vout-p);  
a negative output node (Vout-n);  
first series impedance means (C1, R1) connected between  
said positive input node and said positive output node;  
second series impedance means (C3, R3) connected  
between said negative input node and said negative  
output node;  
first shunt impedance means (R2, C2) comprising a first  
shunt resistor (R2) connected to said positive output  
node and a first shunt capacitor (C2) connecting said  
positive output node to ground;  
second shunt impedance means (R4, C4) comprising a  
second shunt resistor (R4) connected to said negative  
output node and a second shunt capacitor (C4)  
connecting said negative output node to ground;  
and shunt impedance modifying means comprising,  
a first buffer amplifier (A1) having an input  
connected to said positive output node and an output  
connected to a common mode voltage node,  
a second buffer amplifier (A2) having an input  
connected to said negative output node and an output  
connected to said common mode voltage node,*

a first differential amplifier (A3) having a first input connected to said common mode voltage node, a second, opposite-polarity input connected to ground, positive and negative outputs, one of said outputs being connected to a first further shunt capacitor (C5), the other end of said first further shunt capacitor being connected to said positive output node, the other said output being connected to a second further shunt capacitor (C6), the other end of said second further shunt capacitor being connected to said negative output node, and a control signal input for receiving a first control signal controlling the gain of said first differential amplifier, and

a second differential amplifier (A4) having a first input connected to said common mode voltage node, a second, opposite-polarity input connected to ground, positive and negative outputs, one of said outputs being connected to said first shunt resistor (R2), the other end of said first shunt resistor being connected to said positive output node, the other said output being connected to said second shunt resistor (R4), the other end of said second shunt resistor being connected to said negative output node, and a control signal input for receiving a second control signal controlling the gain of said second differential amplifier, whereby the effective shunt impedance of said first and second shunt impedance means can be altered by said first and second control signals".

## Reasons for the Decision

1. The appeal complies with the requirements of Articles 106 to 108 and Rule 64 EPC and is, therefore, admissible.

2. Amendments

Claim 1 is based on the embodiment shown in figure 5 and described in the originally filed description, page 6, line 22 to page 8, line 9.

The board is thus satisfied that the amendments to this claim comply with the requirements of Article 123(2) EPC.

3. Novelty, inventive step

3.1 Document D2 (see figure 1 and corresponding description) is concerned with a differential attenuator and the calibration circuitry for setting the common mode rejection ratio at low and high frequencies, thereby providing the closest prior art. In particular, document D2 discloses a differential attenuator with a positive and negative side. Each attenuator side has input and output nodes, resistors (R1, R2; R5, R6) and capacitors (C1, C2; C5, C6) connected between the input and output node (ie providing "series impedance means" within the meaning of the application under appeal), and resistors (R3, R4; R7, P1) and capacitors (C3, C4; C7, C8) connecting the output node to ground (ie providing "shunt impedance means"). Some of the latter capacitors and resistors are variable so as to allow the alteration of the impedance in order to adjust the

common mode rejection ratio at high and low frequencies, respectively.

The differential attenuator according to claim 1 differs from that shown in document D2 in substance in that the positive and negative output nodes are connected, via buffer amplifiers, to a single node ("common mode voltage node" see figure 5 of the application) and in that two differential amplifiers with controllable gain are provided which are connected to resistors and capacitors of the shunt impedance means, thereby allowing to adjust the effective Miller capacitance and conductance as a function of the gain of the differential amplifiers.

Novelty of the subject-matter of claim 1 is, thus, provided over document D2 (Articles 52(1) and 54(1) and (2) EPC). Novelty is also provided with respect to the remaining available, more remote prior art.

3.2 The differential attenuator according to claim 1 eliminates the manually adjustable components of document D2 and substitutes electronically controllable circuitry therefor, thereby reducing the space required by the circuitry to compensate for common mode rejection ratio errors. Furthermore, by providing a single differential amplifier for simultaneously adjusting, though in opposite senses, the shunt capacitances (or resistance) at both the positive and the negative side of the differential attenuator, a simple and low power circuit is obtained.

As far as the solution offered according to claim 1 is concerned, reference may be made to document D3,

discussed in the originally filed description of the application under appeal (see page 4, lines 16 to 27 and figure 2). From this document the replacement of a manually variable capacitor by a "Miller capacitor", ie a capacitor and an amplifier, is known in the context of a single-ended RC attenuator.

Furthermore, document D1 discloses both an electronically controlled variable capacitor (see figure 2 and corresponding description) comprising a multiplier with controllable gain combined with a capacitor (see in particular the implementation of the variable gain amplifier 35 of figure 7), and an electronically controlled variable resistor (see figure 4 and corresponding description) comprising a multiplier with controllable gain combined with a resistor, in the context of single-ended AC attenuators and specifically in order to avoid bulky discrete components and inconvenient manual adjustments (see column 12, lines 21 to 25).

Neither of these documents, however, addresses a differential attenuator with a positive and a negative side and can be held to render obvious the particular circuitry solution for both sides with only two differential amplifiers as provided by claim 1. The claimed solution is not considered to be rendered obvious by any of the remaining, less relevant prior documents either.

Accordingly, the subject-matter of claim 1 is also considered to involve an inventive step with respect to the available prior art (Articles 52(1) and 56 EPC).



4. The description and drawings have been adapted to the amended claim as appropriate.

## **Order**

### **For these reasons it is decided that:**

1. The decision under appeal is set aside.
2. The case is remitted to the examining division with the order to grant a patent with the following documents:

Claims: No. 1 filed at the oral proceedings on  
16 November 2006;

Description: Pages 1 to 8 filed at the oral  
proceedings on 16 November 2006;

Drawings: Sheets 1/2 and 2/2 filed at the oral  
proceedings on 16 November 2006.

The Registrar:

The Chairman:

R. Schumacher

B. Schachenmann