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Datasheet for the decision of 20 May 2008

Case Number: T 0914/05 - 3.4.03

Application Number: 00915797.5

Publication Number: 1155448

IPC: H01L 23/367

Language of the proceedings: EN

Title of invention:
Leadless Chip carrier design and structure

Patentee:
Skyworks Solutions, Inc.

Opponent:
-

Headword:
-

Relevant legal provisions:
EPC Art. 52(1)

Relevant legal provisions (EPC 1973):
EPC Art. 56

Keyword:
"Inventive step (no)"

Decisions cited:
-

Catchword:
-

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Case Number: T 0914/05 - 3.4.03

D E C I S I O N
of the Technical Board of Appeal 3.4.03
of 20 May 2008

Appellant: Skyworks Solutions, Inc.
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Woburn, Massachusetts 01801 (US)

Representative: Viering, Jentschura & Partner
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Decision under appeal: **Decision of the Examining Division of the European Patent Office posted 19 January 2005 refusing European application No. 00915797.5 pursuant to Article 97(1) EPC.**

Composition of the Board:

Chairman: E. Wolff
Members: R. Q. Bekkering
T. Bokor

Summary of Facts and Submissions

I. This is an appeal against the refusal of application 00 915 797 for lack of an inventive step over

D1: Patent Abstracts of Japan, vol. 1999, no. 02, 26 February 1999 & JP-A-10 313 071 and the corresponding English translation

and inter alia

D4: Mulgaonker S et al., "An Assessment of the Thermal Performance of the PBGA Family", Proceedings of the Annual Semiconductor Thermal Measurement and Management Symposium, San Jose, February 7 - 9, 1995, IEEE, New York, US, pages 17 to 27.

II. Oral proceedings were held in the absence of the appellant applicant, of which the board had been informed in advance.

III. The appellant requested in writing that the decision under appeal be set aside and a patent granted on the basis of claims 1 to 16 filed with the letter dated 15 April 2008.

IV. Claim 1 reads as follows:

"*1. An electronic package (110) for a device (120), comprising*
an interconnect substrate (220) having an upper surface (200) and a lower surface (210);

a die attach bond pad (240) on said upper surface (200) for receiving a semiconductor device chip (100), wherein the die attach bond pad (240) is a metallic pad;

a heat spreader (290) on said lower surface (210), said heat spreader positioned beneath said die attach bond pad (240);

a plurality of vias (250, 255) passing through the thickness of said interconnect substrate (220) from said upper surface (200) to said lower surface (210);

a first group (255) of said vias positioned to intersect both said die attach bond pad (240) and said heat spreader (290);

a second group (250) of said vias positioned about the periphery of and spaced away from said die attach bond pad (240);

a plurality of bond pads (260) positioned on said upper surface (200), each of said plurality of bond pads abutting one of said vias of said second group (250);

a plurality of lands (280) positioned on said lower surface (210), each of said plurality of lands abutting one of said vias of said second group (250); and

an electrically conductive medium located in said second group (250) of vias to electrically interconnect each of said plurality of bond pads (260) to said plurality of lands (280);

a thermally and electrically conductive heat spreader (290) being a metallic pad;

a thermally and electrically conductive medium located in said first group (255) of vias to thermally and electrically interconnect said semiconductor device chip (100) and said heat spreader (290); and

each of said plurality of lands (280) being attached to a printed circuit board (130) by solder;
said die attach bond pad (240) being electrically connected to at least one device electrode (300) on said semiconductor device chip (100) by at least one downbond (295)."

Independent claim 8 is directed to a corresponding semiconductor device.

V. The appellant applicant argued as follows:

The subject-matter of the claims involved an inventive step over the cited prior art.

Document D1 disclosed an electronic package in which the integrated circuit adhered to the upper surface of the interconnect substrate by means of a thermally conductive adhesive. The package of D1 thus lacked the die attach bond pad and the corresponding down bond connecting the die attach bond pad to a device electrode of the semiconductor device chip as per claim 1. Furthermore, D1 disclosed a heat dissipation structure on the lower surface of the interconnect substrate including a heat radiation pattern, an adhesive layer and a radiator plate. In contrast thereto the invention's heat spreader provided a single metallic pad that could be directly soldered to a PCB. Furthermore, according to D1 the heat radiation pattern was "brought to a state in which it is electrically insulated from the bare chip". Moreover, the invention did not require a combination of solder balls and conductive adhesive to attach the lands on the lower surface of the interconnect substrate to the PCB.

The objective technical problem relative to D1 could be seen in providing an electrical package with reduced electrical parasitics and predictable heat dissipation together with an efficient ground.

Document D4 was merely an academic study on the thermal behaviour of a plastic ball grid array (PBGA). The skilled person looking for an improvement of the package with respect to the grounding structure would thus not consider D4. Furthermore D4 was silent on any vias not used for grounding, failed to disclose vias thermally and electrically interconnecting a die attach pad and a heat spreader, and did not disclose a downbond connecting the die with the die pad.

Reasons for the Decision

1. The appeal is admissible.

2. *Novelty*

2.1 *Document D1*

Document D1 discloses a package for a semiconductor device in which the heat emitted by the semiconductor device is dissipated via through holes in the package substrate to a heat radiation pattern on the lower surface of the substrate.

In particular, the electronic package of D1 (see translation of D1, paragraphs [0023] to [0036] and

[0050] to [0052] and figures 1 and 9, respectively) comprises, using the terminology of the application,
- an interconnect substrate (2) having an upper surface (2a) and a lower surface (2b);
- a thermally conductive adhesive (4) on said upper surface (2a) for receiving a semiconductor device chip (3);
- a heat spreader (12) on said lower surface (2b), said heat spreader positioned beneath said die;
- a plurality of vias (through holes) (9, 13) passing through the thickness of said interconnect substrate (2) from said upper surface (2a) to said lower surface (2b);
- a first group (13) of said vias positioned to intersect both said die and said heat spreader;
- a second group (9) of said vias positioned about the periphery of and spaced away from said die;
- a plurality of bond pads (5) positioned on said upper surface (2a), each of said plurality of bond pads abutting one of said vias of said second group (9);
- a plurality of lands (8) positioned on said lower surface (2b), each of said plurality of lands abutting one of said vias of said second group (9); and
- an electrically conductive medium (10) located in said second group (9) of vias to electrically interconnect each of said plurality of bond pads (5) to said plurality of lands (8);
- a thermally and electrically conductive heat spreader (12) being a metallic pad;
- a thermally and electrically conductive medium (14) located in said first group (13) of vias to thermally interconnect said semiconductor device chip (3) and said heat spreader (12); and

- each of said plurality of lands (8) being attached to a printed circuit board (21) by solder, ie solder balls (11) and solder paste (24).

The appellant applicant argued that the invention's heat spreader differed from that of D1 in that it provided a single metallic pad that could be directly soldered to a PCB, whereas D1 provided a heat radiation pattern 12, an adhesive 15 and a radiator plate 16.

The board notes, however, that the "heat radiation pattern" 12 of D1 is formed of a high thermal conductivity metal such as Cu and serves the purpose of transmitting heat emitted by the bare chip (see translation of D1, [0030]). It thus forms a "thermally and electrically conductive heat spreader being a metallic pad" as per claim 1. As to the appellant's argument that the invention's heat spreader provided "a single metallic pad that can be directly soldered to a PCB", it is noted that claim 1 is not limited hereto.

As to the appellant's argument that the invention did not require solder balls and conductive adhesive to attach the lands on the lower surface of the interconnect substrate to the PCB as was the case in D1, it is noted that the bonding by means of solder balls (11) and the conductive adhesive of D1, which is for instance a solder paste (see translation of D1, [0051]), with subsequent reflow, may be subsumed under "being attached ... by solder" as per claim 1.

2.2 Not disclosed in document D1 is the provision of a die pad underneath the semiconductor chip and of a downbond

electrically connecting the die pad to a device electrode of the semiconductor chip.

Accordingly, the subject-matter of claim 1 is new over document D1 (Article 52(1) EPC 2000, Article 54(1) and (2) EPC 1973). The subject-matter of claim 1 is also new over the remaining available, more remote prior art.

3. *Inventive step*

3.1 The provision of a die pad underneath the semiconductor chip of D1, which pad is thermally and electrically conductive and electrically connected to the semiconductor chip, in particular where it is connected to the chip's ground, offers a ground plane close to the chip resulting in reduced parasitic effects such as crosstalk and noise.

The objective problem to be solved relative to document D1, which is considered to provide the closest prior art, is thus to reduce parasitic effects on the semiconductor device.

It is noted that this problem corresponds in substance to that identified by the appellant (see point V above).

No inventive merit is seen in the formulation of this problem, as the skilled person working in the technical field of semiconductor devices at issue would be generally aware that high speed devices require low parasitics, see eg document D4 (page 17, right-hand column, third paragraph).

3.2 Document D4 provides an assessment of the thermal behaviour of PBGA devices. It discloses a semiconductor die mounted on a die pad on the upper surface of a substrate within the package. Vias trough the substrate connect the die pad to a metal heat spreader pad on the bottom layer of the substrate to which thermal bumps are attached (page 17, right-hand column, penultimate paragraph). According to D4, the "*thermal bumps typically double as ground pins*" (page 18, left-hand column, first paragraph). As can be seen from figure 2, the thermal/ground planes and vias within the package are connected to the plane underneath the die forming a die pad, which in turn is electrically connected to the (ground) electrode of the die by a bonding wire.

Hence, as the document is concerned with PBGA packages, as is D1, and relates to planes in the PBGA package both acting as ground planes, and hence for reducing parasitics, and as thermal dissipation planes, in the board's opinion the person skilled in the art concerned with the above problem would consider the document to be relevant.

Moreover, document D4 suggests to the skilled person the use of a thermally and electrically conductive die pad underneath the die providing a ground plane electrically connected to the die by a downbond. Accordingly it would be obvious to the skilled person to adopt this solution to the package of D1, thereby arriving at the subject-matter of claim 1.

3.3 The appellant applicant argued that since according to D1 the heat radiation pattern was "*brought to a state in which it is electrically insulated from the bare*

chip", the skilled person would not consider introducing a ground plate providing an electrical coupling between the chip and the heat spreader.

It is, however, noted that no particular reason is provided in D1 for electrically insulating the radiation pattern from the chip. As would be apparent to the skilled person, such insulation requires special measures. The use of a conventional adhesive which is both electrically and thermally conductive is more straightforward. Accordingly, it would be obvious to the skilled person, where circumstances do not require such electrical insulation, to dispense with it.

Finally, as to the appellant's argument that D4 was silent on any vias not used for grounding, it is implicit that the PBGA of D4 includes further vias, which are not shown, for connecting any remaining electrodes of the die to the correspond balls of the package, as this is an indispensable feature of such packages.

3.4 Hence, the subject-matter of claim 1 is obvious to the person skilled in the art and, therefore, lacks an inventive step in the sense of Article 56 EPC 1973, contrary to Article 52(1) EPC 2000.

3.5 The above applies *mutatis mutandis* to independent claim 8 which is directed to a semiconductor device in substance consisting of the above electronic package including the semiconductor device chip. The subject-matter of claim 8 thus also lacks an inventive step in the sense of Article 56 EPC 1973, contrary to Article 52(1) EPC 2000.

Order

For these reasons it is decided that:

The appeal is dismissed.

Registrar	Chair
S. Sánchez Chiquero	E. Wolff