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Datasheet for the decision of 31 January 2008

Case Number: T 0205/05 - 3.5.04

Application Number: 02721701.7

Publication Number: 1389335

IPC: G11C 11/4097

Language of the proceedings: EN

Title of invention:
Device and method for using complementary bits in a memory array

Applicant:
Micron Technology, Inc.

Headword:
-

Relevant legal provisions:
-

Relevant legal provisions (EPC 1973):
EPC Art. 56
EPC R. 67

Keyword:
"Inventive step - no"
"Decision re appeal - remittal (not applicable)"
"Reimbursement of appeal fee - no"

Decisions cited:
-

Catchword:
-

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Beschwerdekammern | Boards of Appeal | Chambres de recours

Case Number: T 0205/05 - 3.5.04

D E C I S I O N
of the Technical Board of Appeal 3.5.04
of 31 January 2008

Appellant: Micron Technology, Inc.
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Decision under appeal: **Decision of the Examining Division of the European Patent Office posted 17 September 2004 refusing European application No. 02721701.7 pursuant to Article 97(1) EPC.**

Composition of the Board:

Chairman: F. Edlinger
Members: A. Dumont
C. Vallet

Summary of Facts and Submissions

I. The appeal is directed against the decision by the examining division to refuse European patent application No. 02 721 701.7. The application was refused on the ground that the subject-matter of claim 1 lacked an inventive step (Article 56 EPC 1973) in view of a combination of the following prior art documents:

D1: US 4,112,512 A and
D2: WO 97/28532 A1.

II. In a communication accompanying the summons to oral proceedings the board expressed the preliminary opinion that it tended to agree with the analysis set out in the decision under appeal. It further expressed the view that using two DRAM memory cells to store a data bit in a differential or a complementary manner appeared to be textbook knowledge, as evidenced by:

D3: L.A.Glasser et al., "The Design and Analysis of VLSI Circuits", Addison Wesley, 1985, pages 395 to 400.

III. With a letter dated 31 December 2007 the appellant submitted *inter alia* a new set of claims 1 to 13 and pages 1 to 16 of the description of a main request and made the following requests:

(a) As a main request, cancellation of the decision to refuse the subject application is requested and grant of a patent is requested on the basis of the

enclosed claims 1-13 and of the enclosed amended description.

(b) As a first auxiliary request, cancellation of the decision to refuse the subject application is requested and grant of a patent is requested on the basis of only claims 1-6 of the main request and of the enclosed amended description.

(c) As a second auxiliary request, cancellation of the decision to refuse the subject application is requested and remittal to the first instance in the event that the board would be inclined to reject the preceding requests for lack of patentability over D3 taken alone or in combination with other prior art.

(d) In addition, the request for reimbursement of the appeal fee (made in the statement of grounds of appeal) is maintained.

IV. Claim 1 according to the main request and the first auxiliary request reads as follows:

"A method of operating a folded digit line DRAM memory array having a plurality of memory cells wherein, in a plan view, each memory cell having an area less than $8F^2$ comprising:
storing a first bit in a first memory cell of the folded digit line DRAM memory array;
storing a second bit that is complementary to the first bit in a second memory cell of the folded digit line DRAM memory array, wherein the first bit and the second bit *together* form a data bit; *and*

reading the data bit by simultaneously connecting the first memory cell and the second memory cell to a same sense amplifier and
sensing a voltage difference between the first memory cell and the second memory cell by means of the sense amplifier."

(Features added with respect to claim 1 on which the decision under appeal is based have been set in italics.)

V. In a letter dated 25 January 2008 the appellant informed the board that he would not participate in the oral proceedings.

VI. Oral proceedings took place on 31 January 2008 in the absence of the appellant.

VII. The reasons given in the decision under appeal may be summarised as follows.

D1 discloses in figure 2 and in the related description a method of operating a folded digit line DRAM memory array having a plurality of memory cells comprising first and second memory cells for storing complementary first and second bits, the pair of bits together forming a data bit. The feature of claim 1 missing from D1, i.e. the implementation of each memory cell with a layout having an area less than $8F^2$, is known from D2. A combination of the teachings of D1 and D2 to reduce the die size, which is the advantage mentioned in D2, is obvious.

VIII. The appellant's arguments may be summarised as follows:

(a) D1 does not disclose storing complementary values in the pair of memory cells so as to form a "data bit" in the meaning of the invention. Transistors (T9, T10) being only alternately enabled prevent simultaneous reading and sensing of the pair of memory cells in D1. There is also no teaching or incentive in D2 for a combination with D1 to arrive at the claimed invention, which aims to improve the reading and refreshing operations (see page 2, lines 1 to 4 of the present application). The invention is therefore new and inventive.

(b) The appellant disputes the board's interpretation of D3. If D3, which was introduced by the board, was of such a particular relevance, the case should be remitted to the department of first instance following the established case law of the Boards of Appeal.

(c) The appellant acknowledges that the European Patent Convention, strictly read, does not prohibit refusal after the response to a first official communication, with or without warning thereof. However, according to the established case law of the Boards of Appeal and the common practice of the examining divisions as set out in the Guidelines for Examination in the European Patent Office, this should be considered exceptional. In the present case, the applicant's response showed a real effort to deal with the issues raised in the communication and was made in good faith. It should have called for a further

invitation to file observations. A direct refusal after a single communication was therefore premature and reimbursement of the appeal fee under Rule 67 EPC 1973 was justified.

Reasons for the Decision

1. The appeal is admissible.

2. *Main request*

2.1 In comparison with claim 1 on which the decision under appeal is based, the amendments to claim 1 (see features set in italics in paragraph IV above) are supported by the description and drawings (page 14, lines 4 to 10 and 15 to 25; figures 8 and 10) disclosing the simultaneous firing of the gates of the memory cells together forming the data bit, the ensuing charge sharing with their respective digit lines (D0 and D0*) and the comparison of the charges on the digit lines by the sense amplifier.

2.2 The appellant has not disputed the finding in the decision under appeal that D1 discloses in the context of figure 2 a method of operating a folded digit line DRAM memory array having a plurality of memory cells (pairs of cells (C1, T1) and (C2, T2)) and a sense amplifier connected to bit lines (B0, B1).

2.3 The appellant argues that the array in D1 cannot operate so as to form a data bit storing complementary bits in a pair of memory cells in the meaning of the present invention. This argument is not convincing for

the following reasons. Both bit lines in D1 are equalised to a high potential (VH, i.e. 8 volts) during a precharge phase when transistors (T6, T7, T8) are activated (see column 6, lines 30 to 33; column 7, lines 20 to 29). These transistors are however deactivated during a read/write operation (see figure 3: RBL). The pair of memory cells is expressly designated in D1 as being a "two-device storage cell" (see column 5, line 65, to column 6, line 2), in which complementary bit values (ground potential and VH) are stored (see column 6, lines 21 to 26). The two storing steps according to claim 1 are therefore known from D1.

2.4 The appellant further argues that the pair of cells are not read and sensed simultaneously in D1. This argument is also not convincing for the following reasons. During the read operation shown in figure 3 of D1, both cells are simultaneously activated by applying a high voltage on the common word line (WL) for them to share their charge with the precharged bit lines. The voltage difference ("extremely low differential signal", "ΔV") resulting from the charge sharing is sensed and amplified to a full voltage swing by the pre-amplifier (6) constituted by the latched flip-flop (T3, T4, T5) (see column 5, line 44, to column 6, line 12). The switching of the pre-amplifier causes one of the isolating transistors (T9, T10) at the boundary of the memory chip to become conductive (the conducting transistor being "determined solely by the information stored on C1 and C2"), whereas the other one remains non conductive (see column 5, lines 23 to 36, and column 6, lines 33 to 42). This however does not prevent charge sharing with the respective bit lines

and sensing of a voltage difference by the pre-amplifier in the first place.

2.5 In conclusion, D1 discloses the method steps of storing first and second bits, reading the data bit and sensing a voltage difference as specified in claim 1.

2.6 The only difference between the method of claim 1 and the method known from D1 lies in the fact that the method of claim 1 is implemented with each memory cell "having an area less than $8F^2$". The description of the present application mentions that cells having an area less than $8F^2$, for instance an area equal to $6F^2$, have been discussed in the prior art (see page 9, second paragraph and figure 2). The description further explains that areas of $8F^2$ are more commonly used in folded line architecture arrays (page 12, second paragraph) and that memory cells with less than $8F^2$ could be substituted with similar results in the invention because of reduced power consumption (page 15, second paragraph). The present application does not disclose any further technical effects being achieved by applying the method to such memory cells.

2.7 D2 aims at combining the advantages of both folded and open digit line architectures and discloses cells with an area less than $8F^2$ in an otherwise folded digit line array configuration, providing the advantage of size reduction, also for folded digit line memory arrays (see page 3, lines 8 to 12; page 12, lines 25 to 29; page 43, lines 4 to 6, and figure 45).

2.8 The appellant emphasises that the invention allows for a significant increase in the period required between

refreshing cycles, leading to a lower power consumption. This advantage results from the association of two memory cells forming a data bit and supplying a sense amplifier with a double voltage difference (see page 2, lines 1 to 4, and page 15, lines 3 to 23 of the present application) and it is independent of a particular implementation of the memory cells, for instance with an area less than $8F^2$. Since the advantage is inherent to the association of two cells known from D1 (see points 2.3 and 2.4 above), it cannot contribute to an inventive step.

2.9 In view of the above, the board judges that it would have been obvious for a person skilled in the art to resort to memory cells having the layout as disclosed in D2 in an array operating according to the teaching of D1, in order to achieve the same known advantage of size reduction.

2.10 In conclusion, the subject-matter of claim 1 does not involve an inventive step (Article 56 EPC 1973) and the main request is not allowable.

3. First auxiliary request

Claim 1 according to this request is identical to claim 1 according to the main request. Therefore, its subject-matter does not involve an inventive step (Article 56 EPC 1973) for the same reasons, and the first auxiliary request is thus not allowable.

4. *Second auxiliary request*

The second auxiliary request is for "remittal to the first instance in the event that the board would be inclined to reject the preceding requests for lack of patentability over D3 taken alone or in combination with other prior art." Since D3 was not used in the reasoning above, the preconditions of the request are not fulfilled and the request no longer applies.

5. *Request for reimbursement of the appeal fee*

5.1 The appellant regards the refusal by the examining division after a single communication as premature in the present case and requests reimbursement of the appeal fee in accordance with Rule 67 EPC 1973.

5.2 Rule 67 EPC 1973 stipulates as a precondition for reimbursement that the appeal be allowable. It is clear from the wording and purpose of the provision that "allowable" is to be understood in the sense that the board, in substance at least, allows one of the appellant's requests. In the present case, none of the requests could be allowed for the reasons set out in the foregoing sections. The precondition not being met, the request for reimbursement of the appeal fee must be rejected.

Order

For these reasons it is decided that:

1. The appeal is dismissed.

2. The request for reimbursement of the appeal fee is refused.

The Registrar The Chairman

D. Sauter F. Edlinger